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I. Education

- Ph.D., Electrical Engineering, 1988
University of Southern California, Los Angeles, California
Dissertation: Mapping/Matching Algorithms to Mesh Reconfigurable Arrays
Advisor: Professor S.Y. Kung, Department of Electrical Engineering,
Princeton University, New Jersey.
- M.S., Electrical Engineering, 1983
National Taiwan University, Taipei, Taiwan
- B.S., Electrical Engineering, 1981
National Taiwan University, Taipei, Taiwan.

II. Publications

1. Journal Articles

- X. Liang and J.S.N. Jean, "Mapping of Generalized Template Matching onto Reconfigurable Computers," in IEEE Transactions on VLSI Systems, Vol. 11, No. 3, pp. 485-498, June 2003.
- X. Liang, J.S.N. Jean, and K. Tomko, "Data Buffering and Allocation in Mapping Generalized Template Matching on Reconfigurable Systems," in the Journal of Supercomputing, Special issue on Engineering of Reconfigurable Hardware/Software Objects, Vol. 19, No. 1, pp. 77-91, May 2001.
- J.S.N. Jean, X. Liang, B. Drozd, K. Tomko, and Y. Wang, "Automatic Target Recognition with Dynamic Reconfiguration," in Journal of VLSI Signal Processing, Vol. 25, No. 1, pp. 39-53, May 2000.
- J.S.N. Jean, K. Tomko, V. Yavagal, J. Shah, and R. Cook, "Dynamic Reconfiguration to Support Concurrent Applications," in IEEE Transactions on Computers, Special Issue on Configurable Computing, Vol. 48, No. 6, pp. 591-602, June 1999.
- H. Kim and J.S.N. Jean, "Concurrency Preserving Partitioning Algorithm for Parallel Logic Simulation," VLSI Design, Vol. 9, No. 3, pp. 253-270, 1999.
- J. Fernando and J.S.N. Jean, "Processor Array Design with FPGA Area Constraint," in IEEE Transactions on CAD of ICs and Systems, Vol. 18, No. 3, pp. 253-264, March 1999.

- J.S.N. Jean and J. Wang, "Weight Smoothing to Improve Network Generalization," in *IEEE Transactions on Neural Networks*, Vol. 5, No. 5, pp. 752-763, September 1994.
- J. Wang and J.S.N. Jean, "Segmentation of Merged Characters by Neural Networks and Shortest Path," in *Pattern Recognition*, Vol. 27, No. 5, pp. 649-658, May 1994.
- J. Wang and J.S.N. Jean, "Resolving Multifont Character Confusion with Neural Networks," in *Pattern Recognition*, Vol. 26, No. 1, pp. 175-187, January 1993.
- S.Y. Kung, J.S.N. Jean, and C.W. Chang, "Fault-Tolerant Array Processors Using Single-Track Switches," in *IEEE Transactions on Computers*, Vol. 38, No. 4, pp. 501-514, April 1989.
- S.Y. Kung, S.C. Lo, J.S.N. Jean, and J.N. Hwang, "Wavefront Array Processors: From Concept to Implementation," in *IEEE Computer*, Vol. 20, No. 7, pp. 18-33, July 1987.

2. Book Chapters

- J.S.N. Jean and S.Y. Kung, "Array Compiler Design for VLSI/WSI Systems," in *TRANSFORMATIONAL APPROACHES to SYSTOLIC DESIGN*, edited by G.M. Megson, Chapman & Hall, U.K., 1993.
- S.N. Jean and S.Y. Kung, "Fault-Tolerant Rectangular Array Processors via Reconfiguration," in *RECONFIGURABLE MASSIVELY PARALLEL COMPUTERS*, PP. 223-249, edited by Hungwen Li, Prentice Hall, New Jersey, 1991.
- S.Y. Kung, S.N. Jean, S.C. Lo, and P. S. Lewis, "Design Methodologies for Systolic Arrays: Mapping Algorithms to Architectures," in *SIGNAL PROCESSING HANDBOOK*, pp. 145-191, edited by C.H. Chen, Marcel Dekker Inc., New York, 1988.

3. Conference Papers

- F. Wang, J. Jean, and S. Sun, "Aspect Ratio Effects on Reconfigurable Computing," in the *Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, pp. 71-77, June 2005.
- Xinzhong Guo, Jack S. N. Jean, "Design Enumeration of Mapping 2D FFT onto FPGA Based Reconfigurable Computers," in the *Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, pp. 305-306, June 2004.
- J. Jean, X. Guo, F. Wang, L. Song, and Y. Zhang, "A Study of Mapping Generalized Sliding Window Operations on Reconfigurable Computers," in the *Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, pp. 51-57, June 2003.

- J. Jean, X. Liang, X. Guo, H. Zhang, and F. Wang, "Initial Results of GOM (GTM Optimal Mapping)," in the Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms, pp. 146-152, June 2002.
- X. Liang and J. Jean, "Memory Access Scheduling and Loop Pipelining," in the Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms, pp. 183-189, June 2002.
- X. Liang and J.S.N. Jean, "Memory Access Pattern Enumeration in GTM Mapping on Reconfigurable Computers," in the Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms, pp. 8-14, June 2001.
- J.S.N. Jean, G. Dong, H. Zhang, X. Guo, and B. Zhang, "Query Processing with An FPGA Coprocessor Board," in the Proc. of the International Conference on Engineering of Reconfigurable Systems and Algorithms, pp. 22-28, June 2001.
- K. Xue, J.S.N. Jean, and L. Hong, "New Media on the Internet - Instrumentation and Measurement over IP," in the Proc. of International Symposium on Multimedia Information Processing, pp. 432-435, December 2000.
- X. Liang and J.S.N. Jean, "Interface Design for the Mapping of Generalized Template Matching on Reconfigurable Systems," in the Proc. of Parallel and Distributed Processing Techniques and Applications Conference, pp. 159-165, June 2000.
- J.S.N. Jean, X. Liang, and K. Tomko, "Data Buffering and Allocation in Mapping Generalized Template Matching on Reconfigurable Systems," in the Proc. of Parallel and Distributed Processing Techniques and Applications Conference, pp. 1111-1117, June 1999.
- J.S.N. Jean, X. Liang, B. Drozd, and K. Tomko, "Accelerating An IR Automatic Target Recognition with FPGAs," in the Proc. of IEEE Symposium on FPGAs for Custom Computing Machines, pp. 290-291, April 1999.
- H. Kim and J.S.N. Jean, "Parallel Optimistic Logic Simulation with Event Lookahead," in the Proc. of 1998 International Conference on Parallel Processing, pp. 20-27, August 1998.
- J.S.N. Jean, K. Tomko, V. Yavagal, R. Cook, and J. Shah, "Dynamic Reconfiguration to Support Concurrent Applications," in the Proc. of IEEE Symposium on FPGAs for Custom Computing Machines, pp. 302-303, April 1998.
- R. Cook, J.S.N. Jean, J.S. Chen, "Accelerating MPEG-2 Encoder Utilizing Reconfigurable Computing," CERC/VIUF/IEEE Computer Society Workshop on "21st Century Electronic Systems Design: Breakthroughs in Quality and Productivity," University of Dayton, December 1997.

- H. Kim and J.S.N. Jean, "Concurrency Preserving Partitioning (CPP) for Parallel Logic Simulation," in the Proc. of 1996 Workshop on Parallel and Distributed Simulation, pp. 98-105, May 1996.
- J. Fernando and J.S.N. Jean, "Interfacing FPGA/VLSI Processor Arrays," in Proc. IEEE International Conference on Application Specific Array Processors, pp. 230-237, July 1995.
- J. Spillane and J.S.N. Jean, "Mapping Nested Loops to Field Programmable Gate Array Based Systems," in Proc. IEEE National Aerospace and Electronics Conference, pp. 227-231, May 1995.
- J.S.N. Jean, Kefu Xue, and Shailendra Goel, "Pattern Theory for Character Recognition," in Proc. IEEE International Conference on Neural Networks, pp. 4198-4203, June 1994.
- J. Wang and J.S.N. Jean, "Multiresolution Neural Networks for Omnifont Character Recognition," in Proc. IEEE International Conference on Neural Networks, pp. 1588-1593, March 1993.
- J. Wang and J.S.N. Jean, "Segmentation of Merged Characters by Neural Networks and Shortest-Path," in Proc. ACM Symposium on Applied Computing, pp. 762-769, February 1993.
- S.N. Jean, "Reconfigurable Processor Arrays with Two-Track Switches," in Proc. IEEE National Aerospace and Electronics Conference, pp. 434-440, May 1992.
- J. Wang and S.N. Jean, "Automatic Rule Generation for Machine Printed Character Recognition Using Multiple Neural Networks," in Proc. IEEE International Conference on Systems Engineering, pp. 343-346, August 1991.
- S.N. Jean, "Fault-Tolerant Array Processors Using N-and-Half-Track Switches," in Proc. of IEEE International Conference on Application Specific Array Processors, pp. 426-437, September 1990.
- S.N. Jean, "A New Distance Measure for Binary Images," in Proc. of IEEE International Conference on Acoustics, Speech, and Signal Processing, pp. 2061-2064, April 1990.
- S.N. Jean and S.Y. Kung, "Communication Reliability Improvement for WSI Array Processors," in Proc. of IEEE International Conference on Communications, pp. 317.4.1-317.4.5, April 1990.
- S.N. Jean and Y.C. Chan, "Input Representation and Output Voting Considerations for Handwritten Numeral Recognition with Backpropagation," in Proc. of International Joint Conference on Neural Networks, Vol. 1, pp. 408-411, January 1990.

- S.N. Jean, H.C. Fu, and S.Y. Kung, "Yield Enhancement for WSI Array Processors Using Two-and-Half-Track Switches," in Proc. of International Conference on Wafer Scale Integration, pp. 243-250, January 1990.
- S.Y. Kung and S.N. Jean, "Array Compiler Design for VLSI/WSI Systems," in Proc. of International Conference on Systolic Arrays, pp. 663-667, May 1989.
- S.Y. Kung and S.N. Jean, "A VLSI Array Compiler System (VACS) for Array Design," in Proc. of IEEE Workshop on VLSI Signal Processing, pp. 495-508, November 1988.
- S.Y. Kung, S.N. Jean, and C.W. Chang, "Fabrication-Time and Run-Time Fault-Tolerant Array Processors Using Single-Track Switches," in Proc. of International Workshop on Defect and Fault Tolerance in VLSI Systems, 7.2.1-7.2.11, October 1988.
- S.N. Jean, C.W. Chang, and S.Y. Kung, "Graceful degradation schemes for static/dynamic wavefront arrays," in Proc. of International Conference on Parallel Processing, pp. 249-255, August 1988.
- S.C. Lo and S.N. Jean, "Mapping algorithm to VLSI array processors," in Proc. of ICASSP, pp. 2033-2036, April 1988.
- S.Y. Kung, S.N. Jean, and S.C. Lo, "Matching algorithm to array processors," in Proc. of ACM-IEEE Fall Joint Computer Conference, pp. 357-365, October 1987.
- S.Y. Kung, P.S. Lewis, and S.N. Jean, "Canonic and generalized mapping from algorithms to arrays - a graph based methodology," in Proc. of the Hawaii Inter. Conf. on System Sciences, Vol. 1, pp. 124 - 133, January, 1987.
- S.N. Jean and Lin-shan Lee, "An efficient low bit rate speech coder with simplified algorithms for digital speech communications," in Proc. of the Inter. Conf. on Global Communications, pp. 799 - 803, 1983.

III. Research Contracts and Grants

- Principal-Investigator, "Handheld One-Way Voice Communication System," Systran Federal Inc.; from May 2001 to September 2003; \$199,998.
- Principal-Investigator, "Application Accelerating Reconfigurable Computer," Air Force Research Lab/Dayton Graduate Institute; from April 2000 to March 2003; \$128,353. (as part of a \$400,000 effort with University of Cincinnati as the lead institution)
- Principal-Investigator, "Image Processing Card for PC Based Simulators," Systran Federal Inc.; from December 2000 to June 2001; \$23,223.
- Principal-Investigator, "Generalized Template Matching on Reconfigurable Computers," Ohio State Research Challenge Grant; from June 2000 to May 2001; \$17,800.

- Principal-Investigator (with Dr. Guozhu Dong), “Query Optimizing Reconfigurable Computing System,” Systran Federal Inc.; from April 2000 to January 2001; \$33,197.
- Principal-Investigator (with Dr. Karen Tomko), “Speculative Run-Time Reconfiguration,” Defense Advanced Research Projects Agency; from April 1999 to March 2000; \$104,046.
- Principal-Investigator, “Handheld One-Way Voice Communication System,” Systran Federal Inc.; from January 2000 to June 2000; \$32,306.
- Principal-Investigator, “A Design Environment for Reconfigurable Computing,” Ohio State Research Challenge Grant; from June 1999 to June 2000; \$15,000.
- Principal-Investigator (with Dr. Karen Tomko), “A Framework for Speculative Run-Time Reconfiguration,” Defense Advanced Research Projects Agency; from September 1997 to March 1999; \$170,184.
- Principal-Investigator, “Dynamically Reconfigurable Computing,” Ohio State Board of Regents; from July 1998 to June 2000; \$38,786.
- Principal-Investigator (with Dr. Karen Tomko), “A Run-Time Reconfiguration System,” Ohio State Research Challenge Grant; from June 1997 to May 1998; \$35,332.
- Principal-Investigator (with Dr. Kefu Xue), “Automatic Target Recognition Module Evaluation,” AbTech Corporation; from June 4, 1996 to June 3, 1998; \$110,000.
- Co-Investigator (with Oscar Garcia as P.I. and others), “Specialized Communication & Terminal Equipment,” National Science Foundation; from September 1996 to August 1999; \$241,314.
- Co-Investigator (with Oscar Garcia as P.I. and others), “Information Technology Center Infrastructure,” Ohio Board of Regents Fund for Equipment; from March 1996 to February 1999; \$1,610,000.
- Co-Investigator (with R. Jain from OSU as P.I. and others), “OCARNet: Ohio Computing and Communications ATM Research Network,” Ohio Board of Regents Fund for Equipment; from March 1996 to February 1999; \$1,721,730.
- Principal-Investigator (with Dr. Kefu Xue), “Pattern Theory-Based Machine Learning,” AbTech Corporation; from December 15, 1994 to November 30, 1995; \$45,700.
- Co-Investigator (with Dr. Mateen M. Rizki), “Relocatable Target Identification Systems,” Wright Laboratory; from March 18, 1993 to December 20, 1993; \$106,965.
- Principal Investigator, “Laser Imaging and Ranging Processing,” Air Force Office of Scientific Research (AFOSR)/RDL; from January 1, 1993 to December 31, 1993; \$20,000.

- Principal Investigator, “Research Initiation Award: Fault Tolerant Processor Array,” National Science Foundation; from August 1, 1989 to January 31, 1992, \$59,385.
- Principal Investigator (with Dr. Raymond E. Siferd), “Engineering Research Equipment Grant: A VLSI Array Compiler System (VACS) for Array Design,” National Science Foundation; from August 15, 1989 to January 31, 1992; \$24,815.
- Principal Investigator, “Documentation for the Array Compiler VACS,” Hughes Aircraft Company; from November 1, 1989 to December 18, 1989; \$4,605.
- Principal Investigator, “VLSI Array Compilation,” Ohio State Research Challenge Award; from January 1, 1990 to June 30, 1991; \$20,000.

IV. Courses taught at Wright State University

CEG/EE260	- Digital Computer Hardware/Switching Circuits
CEG399	- Object-oriented Programming in C++
CS400/600	- Data Structures and Software Design
CEG411	- Microprocessor-Based System Design
CEG421/621	- Microcomputer Design Project
CEG433/633	- Operating Systems
CEG434/634	- Concurrent Software Design
CEG453/653	- Design of Computing Systems
CEG720	- Computer Architecture
CEG750	- Microprocessors
CEG751	- Microprocessors II
CEG820	- Advanced Computer Architecture

V. Ph.D. Dissertation and M.S. Theses Supervised

1. Ph.D. Dissertation Supervised

- Xuejun Liang, Mapping of Generalized Template Matching on Reconfigurable Computers, 2001.
- Hong Kim, Parallel Logic Simulation of Digital Circuits, 1998.
- Joseph Fernando, Mapping Algorithms to Processor Arrays, 1997.
- Jin Wang, Machine-Printed Character Recognition with Neural Networks, 1993.

2. M.S. Theses Supervised

- Arun Inapakolla, “A Preliminary Study of Mapping A SAT Solver Completely onto FPGA,” 2005

- Anand Arumugam, “Two-Dimensional FFT on FPGAs,” 2004
- Nader Kalantari, “A Hybrid HMM-ANN Approach for Speech Phrase Recognition with Smoothing and Negative Training,” 2003
- Ying Zhang, “Generalized Template Matching on a Virtex II FPGA Board,” 2003
- Xinzhong Guo, “A VHDL Component Library Management Platform,” 2002
- Hua Zhang, “A Code Generator for Generalized Template Matching on Reconfigurable Computers,” 2002
- Rong Zeng, “A VHDL Design Assistant for GTM on Reconfigurable Computers,” 2000
- Nathan Kragick, “Boolean Satisfiability Determination Through Reconfigurable Hardware,” 1999
- Robert Cook, “Accelerating An MPEG-2 Encoder Utilizing Reconfigurable Computing,” 1997
- Niranjana R. Kode, “Image Alignment for Laser Imaging and Ranging System,” 1996
- Shouning Liu, “An Interactive Image Catalog System,” 1996
- Gerald Berry, “A Design Methodology for FPGA-Based Digital Filters,” 1996
- John Holt, “Ranking Images by Content Similarity,” 1995
- Evelyn Beachy, “Utilizing Multi-Processor Boards in A Personal Computer,” 1995
- Michael Greene, “Extensions for the Automatic Parallelization of Code for the Silicon Graphics Power C Analyzer,” 1995
- Steven Houtchen, “Design and Implementation of A Circuit Analyzer System,” 1995
- Shailendra Goel, “Pattern Theory for Character Recognition,” 1994
- John Riehl, “Implementation of the Laser Imaging and Ranging System,” 1994
- Sakul Gupta, “Design and Implementation of a Video I/O Board,” 1994
- Jiahn-An Lu, “Design and Implementation of A Real-Time Image Alignment Board,” 1993
- Abd-Alrazzak Habra, “A Simulator for Fault Tolerant Array Processors,” 1993

- Noshin Kagalwalla, “A Parallel Neural Network Architecture for the Recognition of Handwritten Digits,” 1993
- Scott Bilik, “The Modeling and Simulation of an SIMD Graphics Engine in VHDL,” 1993
- Rong-Fong Hsu, “Converting SunWindows Applications to X Window System Applications: A Case Study,” 1993
- Hemang Mehta, “A Simulator for Real Time Fault Tolerance for Mesh Interconnection Networks,” 1992
- Ray Yang, “Filled Form Processing,” 1992
- Scott Robertson, “A Real-Time Hardware-In-The-Loop Simulation of an Unmanned Aerial Research Vehicle,” 1992
- John Mossing, “Developing a Personal Computer Based Digital Signal Processing System,” 1991
- Hsi-Hui Jang, “Machine-Printed Character Recognition,” 1991
- Jen-Kuan Lee, “BlaFSS: Blank Form Specification System,” 1990
- Yi-Chang Chan, “Handwritten Numeral Recognition with Neural Networks,” 1989

VI. Professional Activities

- Is currently an Associate Editor of the Journal of VLSI Signal Processing
- Served with Dr. Sanjaya Kumar (Honeywell Technology Center) as a co-editor of a special issue on Reconfigurable Computing for the journal VLSI DESIGN, Vol 10, NO. 3, 1999.
- Served as a program committee member of the ERSA Conference in Las Vegas, June, 2001 to 2005.
- Served as a program committee member of the ENREGLE 2000 Workshop in Las Vegas, June 2000.
- Served as a program committee member of the 10th International Conference on Parallel and Distributed Computing and System in 1998.
- Served on the technical program committee of the IEEE 1995 International Conference on Application Specific Array Processors

- Reviewed papers for various journals and conferences
- Participated in 1992 and 1994 U.S. Air Force Summer Faculty Program at Wright Laboratory