

Jack S.N. JEAN
Professor
Department of Computer Science and Engineering
Wright State University
Dayton, Ohio 45435
Phone: 937-775-5106, Fax: 937-775-5133
E-mail: jjean@cs.wright.edu

(i) Professional Preparation

National Taiwan University	Electrical Engineering	B.S., 1981
National Taiwan University	Electrical Engineering	M.S., 1983
University of Southern California	Electrical Engineering	Ph.D., 1988

(ii) Appointments

Wright State University	Professor	2001-present
Wright State University	Associate Professor	1994-2001
Wright State University	Assistant Professor	1988-1994

(iii) Publications

Publications most closely related to the proposed project

- (a) X. Liang and J.S.N. Jean, "Mapping of Generalized Template Matching onto Reconfigurable Computers," in IEEE Transactions on VLSI Systems, Vol. 11, No. 3, pp. 485--498, June 2003.
- (b) X. Liang, J.S.N. Jean, and K. Tomko, "Data Buffering and Allocation in Mapping Generalized Template Matching on Reconfigurable Systems," in the Journal of Supercomputing, Special issue on Engineering of Reconfigurable Hardware/Software Objects, Vol. 19, No. 1, pp. 77--91, May 2001.
- (c) J.S.N. Jean, X. Liang, B. Drozd, K. Tomko, and Y. Wang, "Automatic Target Recognition with Dynamic Reconfiguration," in Journal of VLSI Signal Processing, Vol. 25, No. 1, pp. 39--53, May 2000.
- (d) J.S.N. Jean, K. Tomko, V. Yavagal, J. Shah, and R. Cook, "Dynamic Reconfiguration to Support Concurrent Applications," in IEEE Transactions on Computers, Special Issue on Configurable Computing, Vol. 48, No. 6, pp. 591--602, June 1999.
- (e) J. Fernando and J.S.N. Jean, "Processor Array Design with FPGA Area Constraint," in IEEE Transactions on CAD of ICs and Systems, Vol. 18, No. 3, pp. 253--264, March 1999.

Other significant publications

- (a) H. Kim and J.S.N. Jean, "Concurrency Preserving Partitioning Algorithm for Parallel Logic Simulation," VLSI Design, Vol. 9, No. 3, pp. 253-270, 1999.

- (b) J.S.N. Jean and J. Wang, "Weight Smoothing to Improve Network Generalization," in IEEE Transactions on Neural Networks, Vol. 5, No. 5, pp. 752-763, September 1994.
- (c) J. Wang and J.S.N. Jean, "Segmentation of Merged Characters by Neural Networks and Shortest Path," in Pattern Recognition, Vol. 27, No. 5, pp. 649--658, May 1994.
- (d) J. Wang and J.S.N. Jean, "Resolving Multifont Character Confusion with Neural Networks," in Pattern Recognition, Vol. 26, No. 1, pp. 175-187, January 1993.

(iv) Synergistic Activities

- (a) Developed a research tool to manage the scheduling, allocation, loading, and de-allocation of multiple FPGA chips.
- (b) Developed a research tool to map certain image processing algorithms to FPGA chips.
- (c) Is currently an Associate Editor of the Journal of VLSI Signal Processing
- (d) Served with Dr. Sanjaya Kumar (Honeywell Technology Center) as a co-editor of a special issue on Reconfigurable Computing for the journal VLSI DESIGN, Vol 10, NO. 3, 1999.
- (e) Served as a program committee member of several technical conferences, including ERSA (2001-2004) and CIC (2002 to 2004).

(v) Collaborators and Other Affiliations

(a) Collaborators and Co-editors

Professor Frank Scarpino, Univ. of Dayton; Professor Karen Tomko, Univ. of Cincinnati; Professor Ranga Vemuri, Univ. of Cincinnati; Dr. Sanjaya Kumar, Honeywell Technology Center

(b) Graduate and Postdoctoral Advisors

Professor S.Y. Kung, Princeton University

(c) Thesis Advisor and Post-Graduate Scholar Sponsor

Thirty three former students (4 Ph.D. and 31 M.S. students): Xuejun Liang, Hong Kim, Joseph Fernando, Jin Wang, Arun Inapakolla, Anand Arumugam, Nader Kalantari, Ying Zhang, Xinzhong Guo, Hua Zhang, Rong Zeng, Nathan Kragick, Robert Cook, Niranjan R. Kode, Shouning Liu, Gerald Berry, John Holt, Evelyn Beachy, Michael Greene, Steven Houtchen, Shailendra Goel, John Riehl, Sakul Gupta, Jiahn-An Lu, Abd-Alrazzak Habra, Noshin Kagalwalla, Scott Bilik, Rong-Fong Hsu, Hemang Mehta, Ray Yang, Scott Robertson, John Mossing, Hsi-Hui Jang, Jen-Kuan Lee, Yi-Chang Chan