



SAIYU REN, Ph.D.

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Wright State University
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EDUCATION

Degree	Institution	Date
Ph.D.	Wright State University	2008
M.S.	Wright State University	2001
M.S.	Chinese Academy of Sciences	1988
B. S.	South China University of Technologies	1985

PROFESSIONAL EXPERIENCE

Institution	Position	Dates
Wright State University	Assistant Professor	09/2009-present
Wright State University	Visiting Assistant Professor	09/2008-08/2009
Wright State University	Senior Research Associate	03/2001-8/2008
Wright State University	Visiting Scholar	08/1998-02/2001
Shenzhen University	Assistant Professor	03/1993-08/1998
Shenai Semiconductor Co.	Test Engineer	06/1988-03/1993

PROFESSIONAL MEMBERSHIPS

Association	Status
Institute of Electrical & Electronics Engineers (IEEE)	Member
Phi Kappa Phi	Member

PROFESSIONAL AWARDS

Title of Award	Granting Association	Dates
Excellent Student Advisor Award	Shenzhen City Government	1997
Excellent Teaching Award	Shenzhen University	1994-1997
Second Place Award for Education Research	Shenzhen University	1996

TEACHING

Course Taught	Title	No. of Time
EE759	RF CMOS Integrated Circuit Design	1
EE758	CMOS Analog Integrated Circuit Design	2
EE454	VLSI Systems Design	2
EE459	IC Design Synthesis with VHDL	3

M.S. Thesis Supervised	Graduation Date
1. Paesol Veerakitti	06/2010
2. Vinayashree Hirmath	11/2010

M.S. Thesis Supervising

1. Tri Nygun
2. Steven Billman
3. Prashanth Muppala
4. Lawrence David Burich

Ph.D. Dissertation Supervising

1. Vinayashree Hiremath
2. Jian Chen
3. Chris Benedik

SCHOLARSHIP

Articles

1. S. Ren, R. Siferd. "1GS/s Pipelined Delta Sigma Modulator ADC using Residue Averaging Technique", Analog Integrated Circuits and Signal Processing Journal 54, pp. 31-44, January 2008.
2. B. Cheah, S. Ren, R. Siferd, "Design Algorithm and Hardware Implementation of FIR Compensation Filter Implemented in 0.13um CMOS Technology", WSEAS Transactions on Circuits and Systems, Issue 12, Vol 4, pp. 1421-1433, December 2005.
3. S. Ren W. Zhou., "Development of Automatic Controlled Sterilizing Equipment with Pulsed Light," Food and Machine 97(5).
4. S. Ren, D. Xi., "Study on the Influence of Pulsed Light on Food Ingredients and Food Preservation," Journal of Shenzhen University (Science &Engineering), 1995 (4).

U. S. Patents

1. R. Siferd and S. Ren, "Pipelined Delta Sigma Modulator Analog to Digital Converter", Provisional Patent Application, April 25, 2006.

Papers Published in Full and Official Proceedings

1. S. Ren and R. Siferd, "CMOS 1.6 GHz Bandwidth 12 Bit Time Interleaved Pipelined ADC", IEEE International Conference on Information Technology, Las Vegas, Nevada, April, 2011.
2. V. Hiremath, S. Ren, "A 6-bit Low Power Folding and Interpolating ADC", IEEE Instrumentation and Measurement Technology Conference (I2MTC 2011), Hongzhou, China , May 2011.
3. G. Y. Lee, S. Ren, S. N. Kim and R. R. Naik "A Tunable CMOS Read-out Integrated Circuit for Carbon Nanotube-based Bio-sensors", IEEE Instrumentation and Measurement Technology Conference (I2MTC 2011), Hongzhou, China , May 2011.
4. V. Hiremath, S. Ren, "An Ultra high speed encoder for flash A/D converters", IEEE Instrumentation and Measurement Technology Conference (I2MTC 2010), Austin, Texas , May 2010
5. S. Ren, R. Siferd, "PERFORMANCE COMPARISON OF TWO LOW POWER WIDE TUNING RANGE VCOS IN 90 NM CMOS" IEEE International SOC Conference, Northern Ireland, UK, Sep. 2009
6. S. Ren, R. Siferd, "A 7.8 GHz CMOS PLL VCO", IASTED International Conference on Circuit and System (CS 2008), Kona-Kohala, Hawaii, Aug. 2008.
7. S. Ren, R. Siferd, " Flexible RF Band Pass Analog to Digital Converter For Multi-Channel Receivers", Circuits, Signals and Systems (CSS), Banff Canada, July 2007.
8. S. Ren, R. Siferd, Robert Blumgold, Nima Emami, "Pipelined Delta Sigma Moduator Analog to Digital Converter, IEEE Midwest Circuits and Systems Symposium, San Juan, P.R., August, 2006.
9. S. Ren, R. Siferd, R. Blumgold, "Hardware Efficient FIR Compensation Filter for Delta Sigma Analog to Digital Converters" IEEE Midwest Circuits and Systems Symposium , Cincinnati, OH, August, 2005.
10. S. Ren, R. Siferd, and R. Blumgold, "Parallel Time Interleaved Delta Sigma Band Pass Analog to Digital Converter for SOC Applications", IEEE International System on Chip Conference, Santa Clara, CA, September, 2004

11. M. Myers, S. Ren, M. Wang, and R. Siferd “Broadband Delta Sigma Modulator with 1 GHz Sampling Rate and 4 Bit Quantizer in 0.18um CMOS Technology” NASA Symposium on VLSI Design, Coeur d’Alene, Idaho, May, 2003
12. R. Siferd, S. Ren, T. Grimes, R. Blumgold, C. Cerny, and T. Chang, “100 MHz Delta Sigma Modulator with 4-Bit Quantizer in 0.35um CMOS Technology” The 2002 International Multiconference in Computer Science, VLSI ‘02, Las Vegas, Nevada, June, 2002.

Technical Reports

1. R. Siferd, J. Emmert, S. Ren, “Antijam (AJ) Processing Application Specific Integrated Circuits (ASIC) for Hand-Digital held Global Positioning Satellite (GPS) Receiver”, Phase II Final Report, Air Force Research Laboratory, March 2011.
2. R. Siferd, and S. Ren, “Digital Synthesizer with Tuning Filter for Advanced Electroni Warfare (EW) Application”, Phase I Final Report, Air Force Research Laboratory, July 2009.
3. S. Ren and R. Siferd, “Advanced CMOS IF Stage”, Final Report, Raytheon RF Component, June 2009.
4. R. Siferd, J. Emmert, S. Ren, “Antijam (AJ) Processing Application Specific Integrated Circuits (ASIC) for Hand-Digital held Global Positioning Satellite (GPS) Receiver”, Phase I Final Report, Air Force Research Laboratory, November 2008.
5. R. Siferd, S. Ren, B. Rigling, J. Wu,, “Non-coherent Dual Platform Advanced Mono-pulse Countermeasures (AMC) Standoff Jammer”, Phase I Final Report, Air Force Research Laboratory, March 2008.

Grants Funded

1. Co-PI: S. Ren, Y. Zhuang “Deployable Low Power Carbon-Nanotube Sensors”, USAF/AFMC DET 1 AF Research Laboratory, RSP# 667885, 12/2/09—4/30/11, \$200,000
2. PI, Phase II “Digital Synthesizer with Tuning Filter”, RBS Technologies, LLC, RSP#667909, 11/25/09—11/24/2011, \$199,997.
3. PI, Phase II “Multi Channel RFASIC for Handheld GPS Receiver Anti Jam Enhancement”, RBS Technologies, LLC, RSP# 667654, 4/8/09-10/14/11, \$200,000.
4. Contributor, PI: John Emmert, Phase II “Anti-jam ASIC for Handheld GPS”, RBS Technologies, LLC, RSP#667409, 7/08—2/11, \$200,000.
5. PI, “Advanced CMOS IF Receiver Stage, Phase III”, Raytheon RF Components, RSP# 667449 8/08—06/09, \$70,000.
6. PI, Phase I “Digital Synthesizer with Tuning Filter”, RBS Technologies, LLC, RSP#667504, 11/11/08—09/10/09, \$30,000

Contributed to the following WSU Research Contracts

1. “Multi Channel RFASIC for Handheld GPS Receiver Anti Jam Enhancement”, RBS Technologies, March 2008-November 2008, \$33,000.
2. “Advanced CMOS IF Receiver Stage, Phase II”, Raytheon RF Components, Jan 2007-Sept 2007, \$60,000
3. “Advanced CMOS IF Receiver Stage, Phase I”, Raytheon RF Components, December 2005-December 2006, \$102,000
4. “High Speed Read Out Integrated Circuit (ROIC) for IR Focal Plane Array Phase II”, RNET Technologies, April 2006-October 2008, \$300,000
5. “High Speed Read Out Integrated Circuit for IR Focal Plane Array Phase I”, RNET Technologies, May 2005-Dec 2005, \$33,000
6. “Wideband Array Analog to Digital Converter”, Systran Federal Corporation, June 2004-June2007, \$330,000.
7. “Pipelined Delta Sigma Analog to Digital Converter”, Systran Federal Corporation, May 2003-Oct 2005, \$300,000.

8. "High Speed/Resolution Parallel Time Interleaved Delta Sigma Analog to Digital Converter", Systran Federal Corporation, May 2001-May 2003, \$353,000.
9. "Parallel Sub-sampling Analog to Digital Converter," Systran Federal Corporation, June 2002 - March 2003, \$33,000.
10. "Radiation Hardened Analog to Digital Converter, Systran Federal Corporation," April 2001 - January 2002, \$33,000.
11. "Analog to Digital Converter Development," Systran Federal Corporation, April 2001 - January 2002, \$33,000.

SERVICE

Department Committees

	Position	Dates
Graduate Studies	Member	2009--now
Undergraduate Study	Member	2010--now

Other Committees

	Position	Dates
WSU STEMM organization	Member	2010-now

Professional Service

1. Reviewer, 2011 IEEE International Conference on Information Technology.
2. Reviewer, IEEE Sensor Journal.
3. Reviewer, IEEE Transactions on Circuits and Systems II
4. Reviewer, IEEE Transactions on Instrumentation & Measurement