Wright State University

EE480/680
Micro-Electro-Mechanical Systems (MEMS)
Summer 2006

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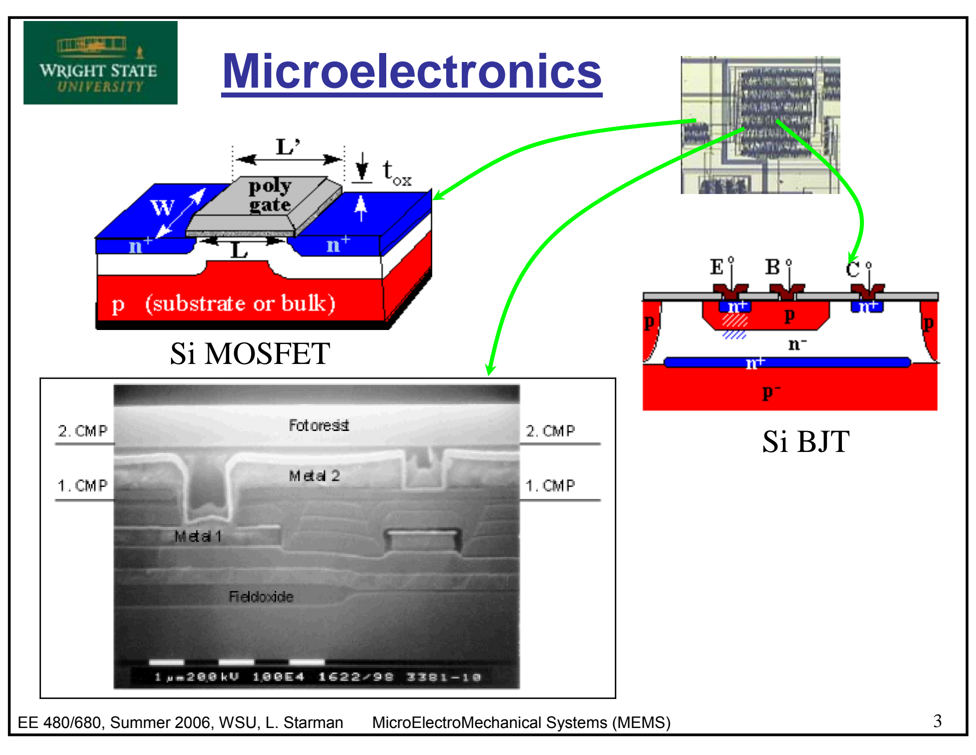
Microelectronics/MEMS

IBM

- How are they made?
- What are they made out of?
- How do their materials behave?

Wires

Transistors
Diodes
Resistors
Capacitors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Microelectronics
L'
t_{ox}
poly gate
W
n+
L
n+
p (substrate or bulk)
Si MOSFET
E
B
C
n+
p
n+
p
p
n-
n+
p-
Si BJT
2. CMP
Fotoresist
2. CMP
1. CMP
Metal 2
1. CMP
Metal 1
Fieldoxide
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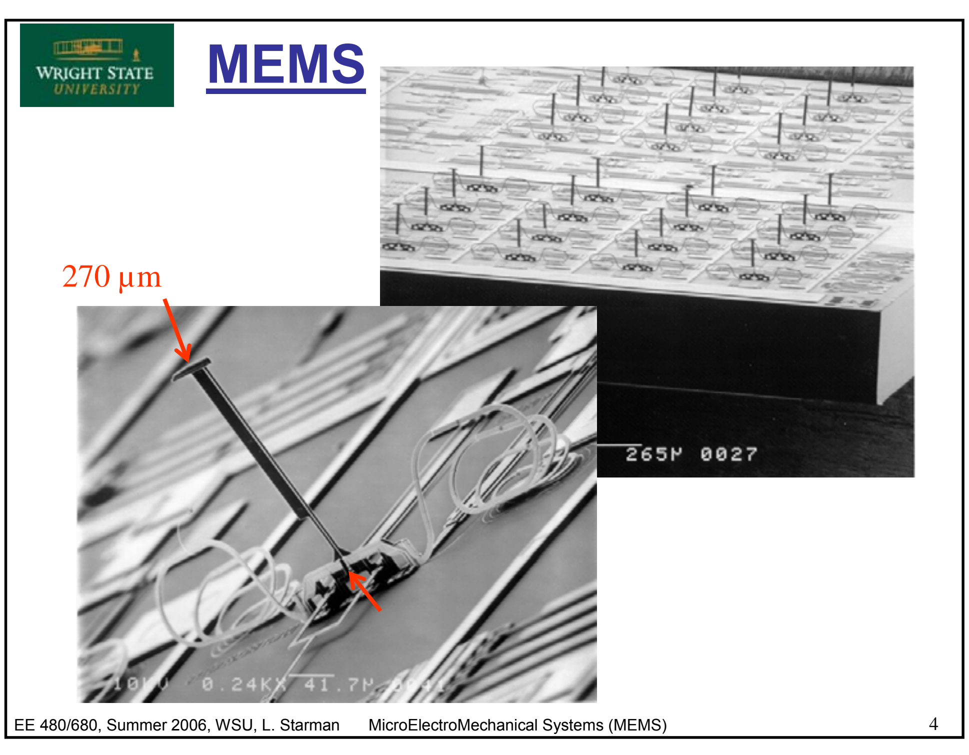
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MEMS
270 µm
265µ 0027
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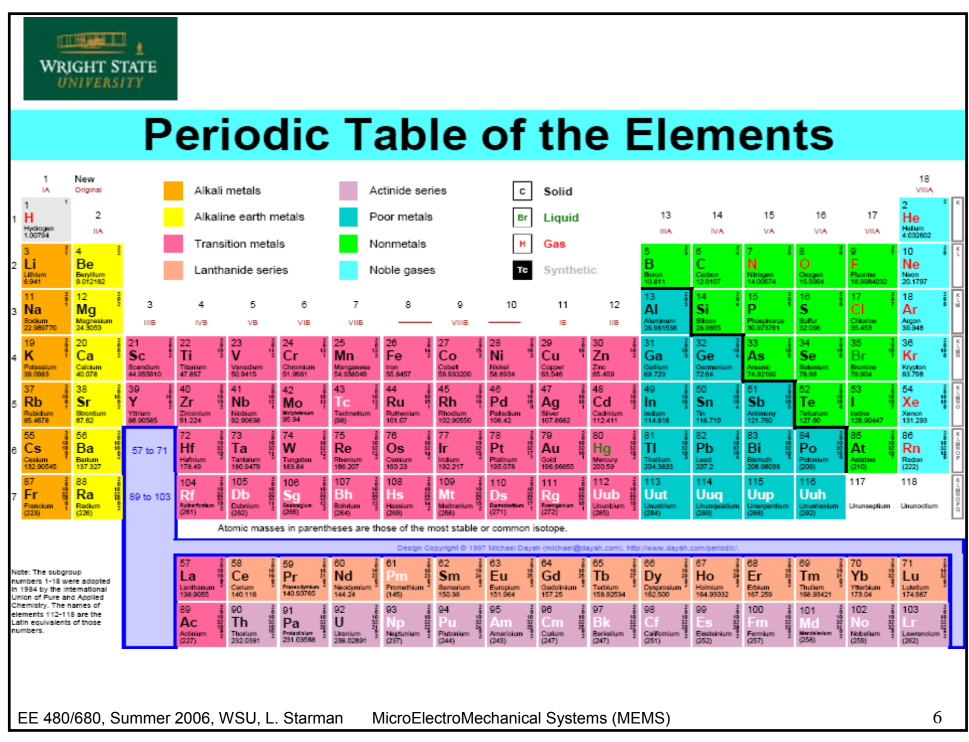
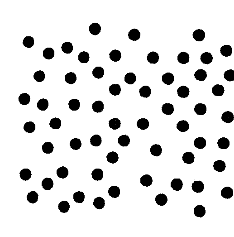
Course Outline

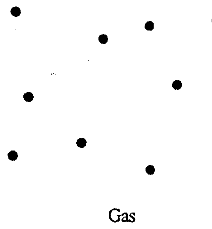
- Semiconductor Materials
- Crystal structure, growth, & epitaxy
- Film formation – oxidation & deposition
- Metalization
- Lithography & etching
- Impurity doping – diffusion & implantation
- Lithography
- Etching
- Resistivity Measurement
- Other Techniques



Semiconductor Materials

- Material Classes
  - Solid
    - Insulators
    - Semiconductors
    - Conductors
  - Liquid
  - Gas





Gas

2-D schematic representation of crystalline solids, amorphous materials or liquids, and gases.

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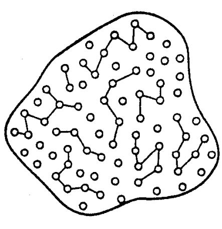
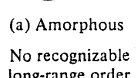
Solids

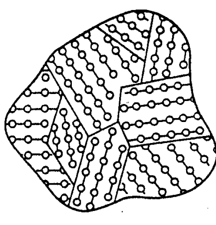
General classification of solids based on the degree of atomic order



(a) Amorphous

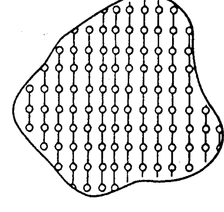


No recognizable long-range order



(b) Polycrystalline

Completely ordered in segments



(c) Crystalline

Entire solid is made up of atoms in an orderly array

- Semiconductors are sensitive to:
  - Temperature, photon flux (illumination), magnetic field, pressure
  - Variability controlled by selectively adding impurities on the order of 1ppm
- **Lattice** – the periodic arrangement of atoms in a crystal

Compound Semiconductors

NOTE: We will concentrate primarily on Si - most common MEMS material

Reasons for Silicon usage:
- Room Temp performance - good
- High quality silicon dioxide
  - Grown thermally
- Reduced cost
- 2nd most abundant element on earth
  - Oxygen first
- Earth's crust
  - Silica & silicates
  - 25%

Compound semiconductor usage:
- Binary
- Ternary
- Quaternary
- Better electrical & optical properties
- Good for
  - High-speed electronics
  - Photonic devices

TABLE 2 Semiconductor Materials[a]

General Classification		Semiconductor Symbol	Semiconductor Name
Element		Si	Silicon
		Ge	Germanium
Binary compound			
	IV-IV	SiC	Silicon carbide
	III-V	AlP	Aluminum phosphide
		AlAs	Aluminum arsenide
		AlSb	Aluminum antimonide
		GaN	Gallium nitride
		GaP	Gallium phosphide
		GaAs	Gallium areside
		GaSb	Gallium antimonide
		InP	Indium phosphide
		InAs	Indium arsenide
		InSb	Indium antimonide
	II-VI	ZnO	Zinc oxide
		ZnS	Zinc sulfide
		ZnSe	Zinc selenide
		ZnTe	Zinc telluride
		CdS	Cadmium sulfide
		CdSe	Cadmium selenide
		CdTe	Cadmium telluride
		HgS	Mercury sulfide
	IV-VI	PbS	Lead sulfide
		PbSe	Lead selenide
		PbTe	Lead telluride
Ternary compound		$Al_xGa_{1-x}As$	Aluminum gallium arsenide
		$Al_xIn_{1-x}As$	Aluminum indium arsenide
		$GaAs_{1-x}P_x$	Gallium arsenic phosphide
		$Ga_xIn_{1-x}As$	Gallium indium arsenide
		$Ga_xIn_{1-x}P$	Gallium indium phosphide
Quaternary compound		$Al_xGa_{1-x}As_ySb_{1-y}$	Aluminum gallium arsenic antimonide
		$Ga_xIn_{1-x}As_{1-y}P_y$	Gallium indium arsenic phosphide

Crystal Structure

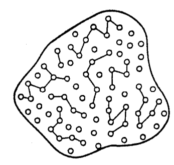
- Elemental semiconductors (column IV)
  - Ex. Si ≡ SiO_2 – very stable oxide (hydrophobic) moderate n_i

    Ge ≡ oxides are soluable to H_2O – large leakage currents as Temp ↑
- Compound Semiconductors (column III-V, II-VI, etc)
  - Ex. GaAs ≡ no stable oxide but direct bandgap

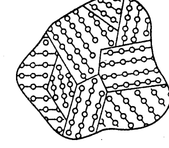
    Applications: microwave and photonic devices

Crystal Structure

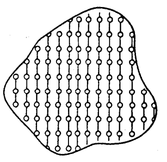
- Arrangement of atoms that define a particular material
- 3 Categories
  - Amorphous – density varies, no unique pattern
  - Crystalline – one region defines all regions
  - Polycrystalline – sets of crystalline regions with boundaries



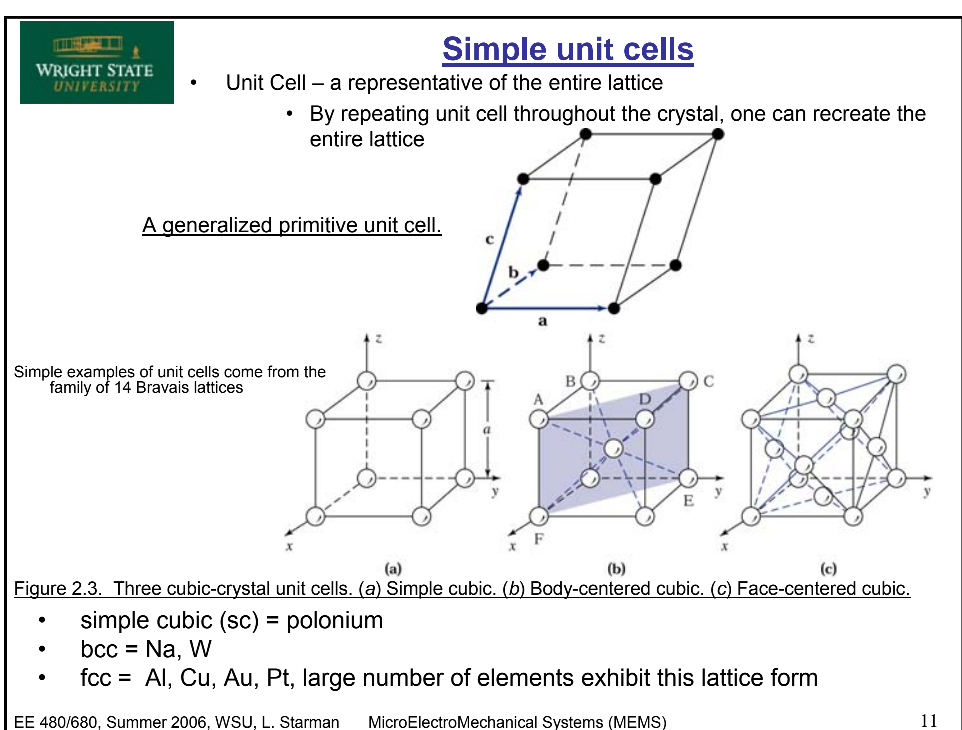
(a) Amorphous



(b) Polycrystalline



(c) Crystalline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Simple unit cells
• Unit Cell – a representative of the entire lattice
• By repeating unit cell throughout the crystal, one can recreate the entire lattice
A generalized primitive unit cell.
c
b
a
Simple examples of unit cells come from the family of 14 Bravais lattices
Figure 2.3. Three cubic-crystal unit cells. (a) Simple cubic. (b) Body-centered cubic. (c) Face-centered cubic.
• simple cubic (sc) = polonium
• bcc = Na, W
• fcc = Al, Cu, Au, Pt, large number of elements exhibit this lattice form
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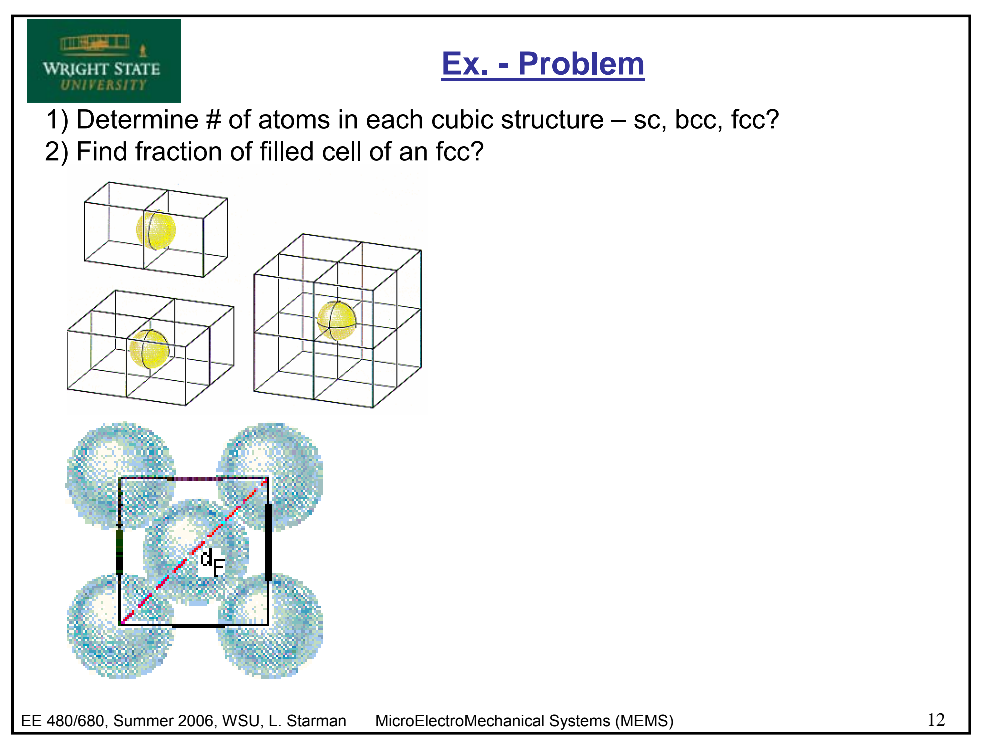
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Ex. - Problem
1) Determine # of atoms in each cubic structure – sc, bcc, fcc?
2) Find fraction of filled cell of an fcc?
dF
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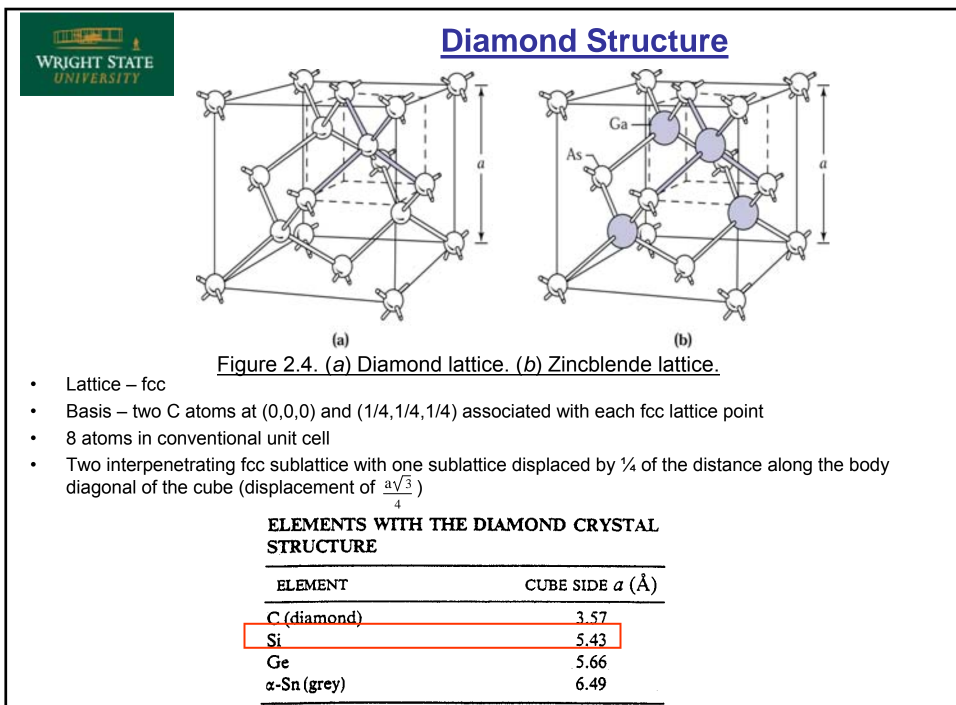
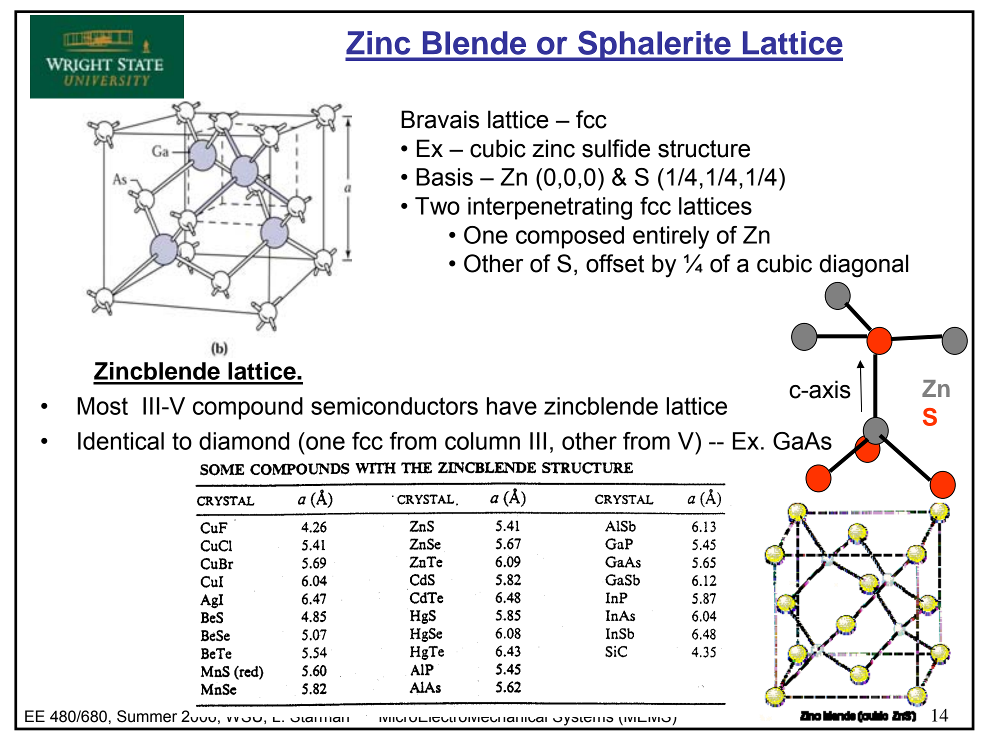
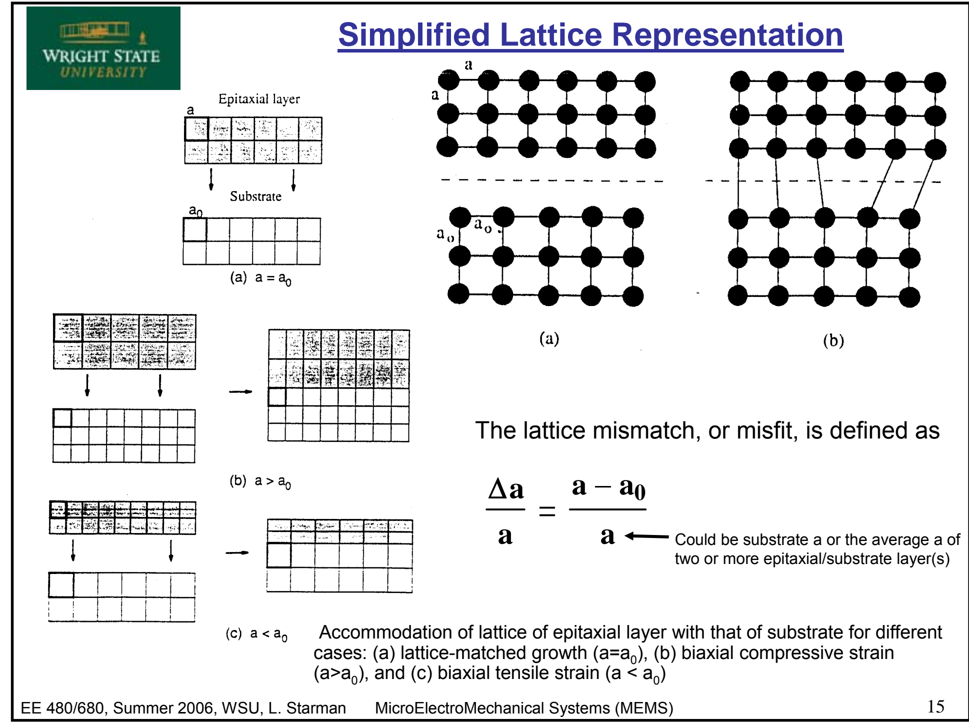


ELEMENT	CUBE SIDE a (Å)
C (diamond)	3.57
Si	5.43
Ge	5.66
α-Sn (grey)	6.49



CRYSTAL	a (Å)	CRYSTAL	a (Å)	CRYSTAL	a (Å)
CuF	4.26	ZnS	5.41	AlSb	6.13
CuCl	5.41	ZnSe	5.67	GaP	5.45
CuBr	5.69	ZnTe	6.09	GaAs	5.65
CuI	6.04	CdS	5.82	GaSb	6.12
AgI	6.47	CdTe	6.48	InP	5.87
BeS	4.85	HgS	5.85	InAs	6.04
BeSe	5.07	HgSe	6.08	InSb	6.48
BeTe	5.54	HgTe	6.43	SiC	4.35
MnS (red)	5.60	AlP	5.45		
MnSe	5.82	AlAs	5.62		



Miller Indices

Cubic lattices (hkl) ≡ crystal plane

A convenient method of defining the various planes in a crystal is to use Miller indices. These indices are obtained using the following steps:

- (1) Find the intercepts of the plane on the three Cartesian coordinates in terms of the lattice constant
- (2) Take the reciprocals of these numbers and reduce them to the smallest three integers having the same ratio
- (3) Enclose the result in parentheses (hkl) as the Miller indices for a single plane

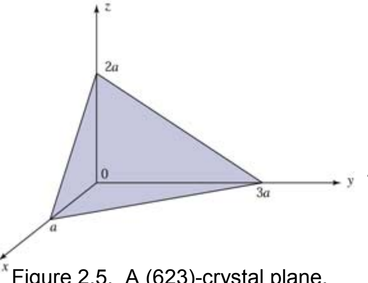


Figure 2.5. A (623)-crystal plane.

Used to define planes & directions in a crystal lattice

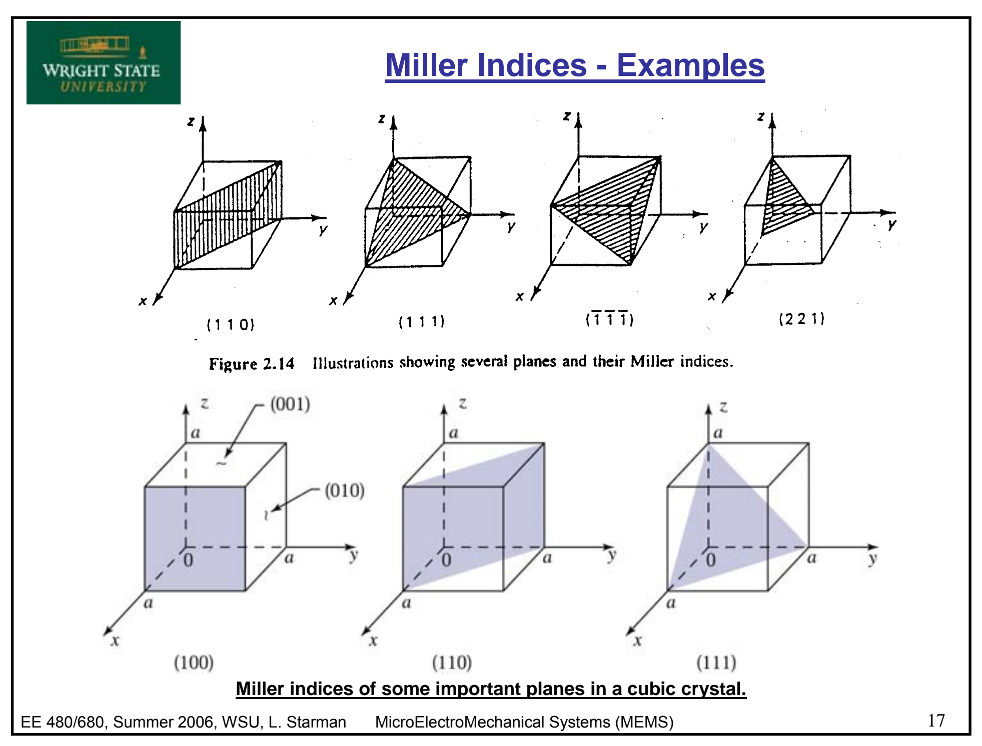
(hkl) plane that intercepts reciprocals of indices

<hkl> ⊥ to (hkl) plane

[hkl] – specific direction

{hkl} – sets of equivalent planes

<hkl> - sets of equivalent directions


Miller Indices - Examples
(1 1 0)
(1 1 1)
(1̄ 1̄ 1̄)
(2 2 1)
Figure 2.14 Illustrations showing several planes and their Miller indices.
(001)
(010)
(100)
(110)
(111)
Miller indices of some important planes in a cubic crystal.
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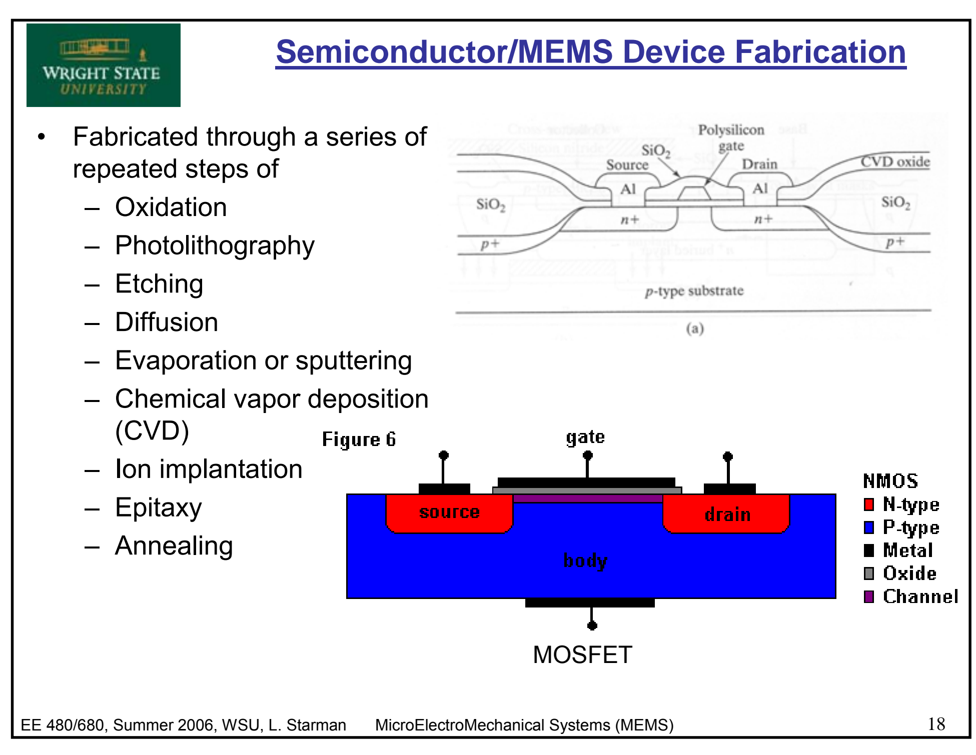
Semiconductor/MEMS Device Fabrication
• Fabricated through a series of repeated steps of
– Oxidation
– Photolithography
– Etching
– Diffusion
– Evaporation or sputtering
– Chemical vapor deposition (CVD)
– Ion implantation
– Epitaxy
– Annealing
Polysilicon gate
SiO2
Source
Drain
CVD oxide
Al
n+
p+
p-type substrate
(a)
Figure 6
gate
source
drain
body
NMOS
N-type
P-type
Metal
Oxide
Channel
MOSFET
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Crystal Growth - Si

Crystal Growth → Two Techniques
- Bridgman
- Czochralski

Si crystal growth from the Melt
- 90% Si crystals grown with Czochralski
- Pure form of sand (SiO_2) – quartzite

$$SiC(s) + SiO_2(s) \rightarrow Si(s) + SiO(g) + CO(g)$$

- Results in metallurgical grade Si – 98% pure
- Si pulverized & treated with HCl to form trichlorosilane

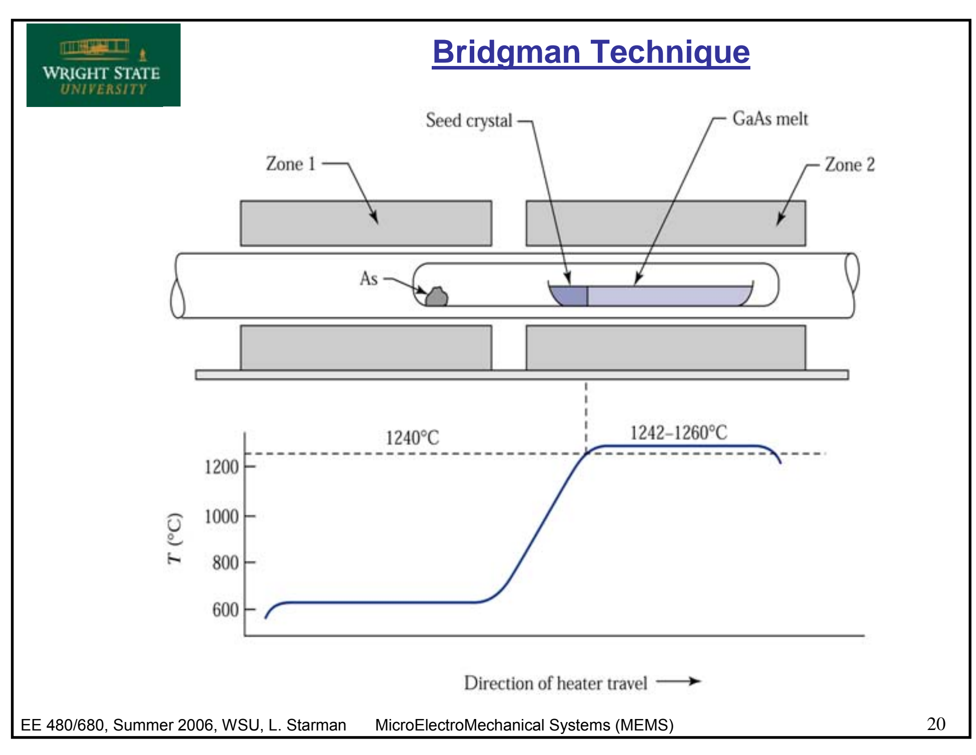
$$Si(s) + 3HCl(g) \xrightarrow{300^{o}C} SiHCl_3(g) + H_2(g)$$

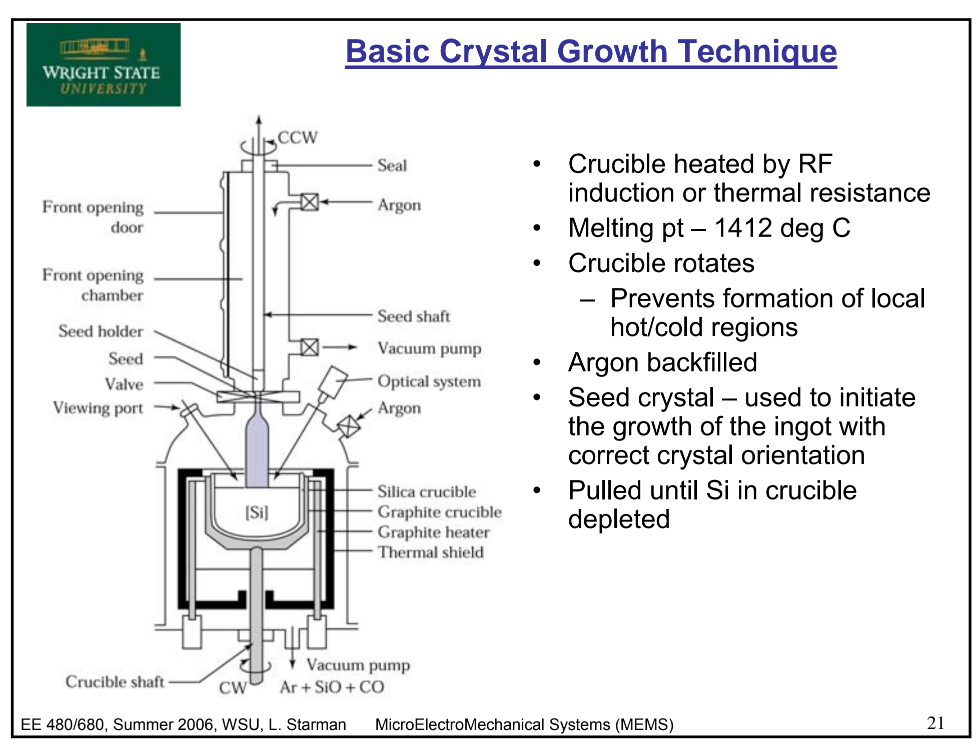
- Trichlorosilane liquid at RT. Fractional distillation of liquid removes unwanted impurities
- Purified SiHCl3 used in hydrogen reduction to prepare the electronic-grade Si

$$SiHCl_3(g) + H_2(g) \rightarrow Si(s) + 3HCl(g)$$

- Pure EGS – impurity concentrations in parts/Billion

Bridgman Technique





Basic Crystal Growth Technique
CCW
Seal
Argon
Front opening door
Front opening chamber
Seed shaft
Seed holder
Seed
Vacuum pump
Valve
Optical system
Viewing port
Argon
[Si]
Silica crucible
Graphite crucible
Graphite heater
Thermal shield
Crucible shaft
CW
Vacuum pump
Ar + SiO + CO
Crucible heated by RF induction or thermal resistance
Melting pt – 1412 deg C
Crucible rotates
– Prevents formation of local hot/cold regions
Argon backfilled
Seed crystal – used to initiate the growth of the ingot with correct crystal orientation
Pulled until Si in crucible depleted
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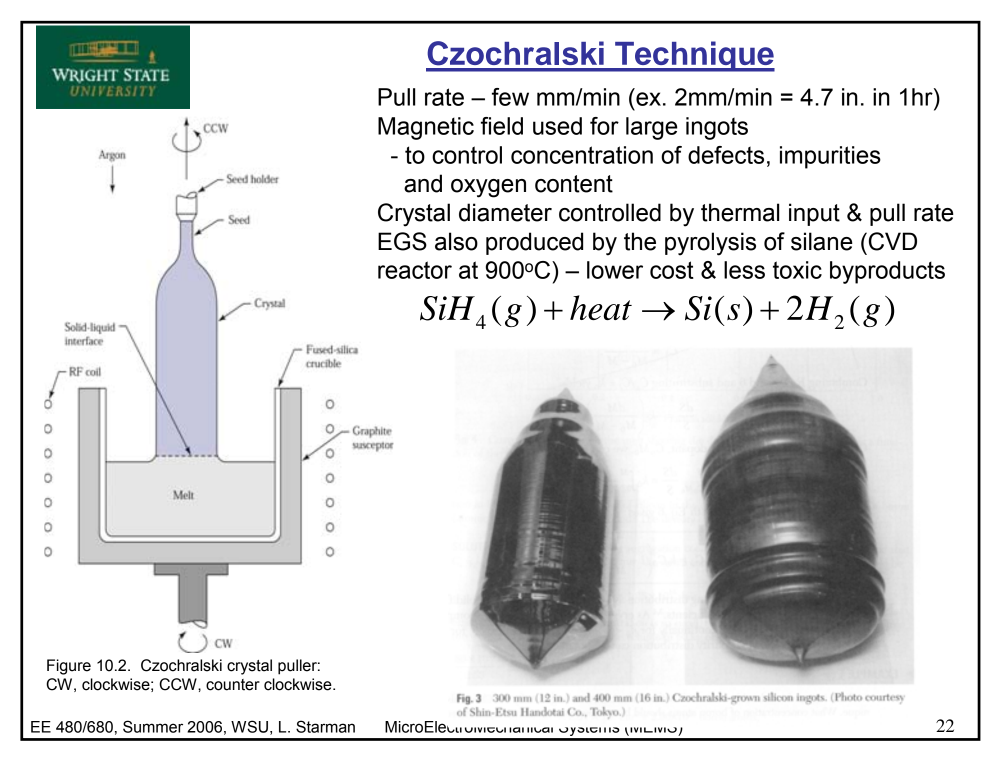

Czochralski Technique
Pull rate – few mm/min (ex. 2mm/min = 4.7 in. in 1hr)
Magnetic field used for large ingots
- to control concentration of defects, impurities and oxygen content
Crystal diameter controlled by thermal input & pull rate
EGS also produced by the pyrolysis of silane (CVD reactor at 900°C) – lower cost & less toxic byproducts
$SiH_4(g) + heat \rightarrow Si(s) + 2H_2(g)$
CCW
Argon
Seed holder
Seed
Crystal
Solid-liquid interface
Fused-silica crucible
RF coil
Graphite susceptor
Melt
CW
Figure 10.2. Czochralski crystal puller: CW, clockwise; CCW, counter clockwise.
Fig. 3 300 mm (12 in.) and 400 mm (16 in.) Czochralski-grown silicon ingots. (Photo courtesy of Shin-Etsu Handotai Co., Tokyo.)
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Distribution of Dopant

For Si – most common dopants
- Boron – p-type
- Phosphorous – n-type

As crystal is pulled from melt, dopant concentration in solid is usually different than the melt at the interface.
Ratio of these two concentrations is defined as the equilibrium segregation coefficient k_o

$$k_0 \equiv \frac{C_s}{C_l} \quad (4)$$

where C_s and C_l are concentrations of solute (by weight) in solid and liquid

TABLE 1 Equilibrium Segregation Coefficients for Dopants in Si

Dopant	k_0	Type	Dopant	k_0	Type
B	8×10^{-1}	*p*	As	3.0×10^{-1}	*n*
Al	2×10^{-3}	*p*	Sb	2.3×10^{-2}	*n*
Ga	8×10^{-3}	*p*	Te	2.0×10^{-4}	*n*
In	4×10^{-4}	*p*	Li	1.0×10^{-2}	*n*
O	1.25	*n*	Cu	4.0×10^{-4}	—[a]
C	7×10^{-2}	*n*	Au	2.5×10^{-5}	—[a]
P	0.35	*n*			

[a]Deep-lying impurity level.

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Float Zone Process

- Ideal for crystal purification
- High purity cast polysilicon rod
- A small zone (~ few cm) is heated by RF heater
- Floating zone traverses rod – molten Si is held in place by surface tension
- No contamination from crucible

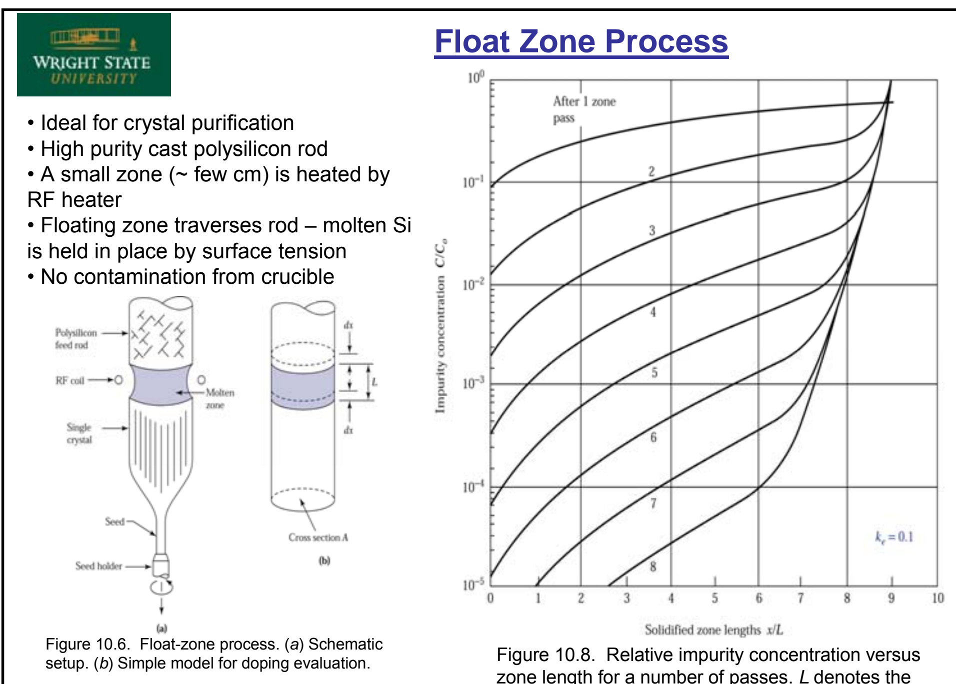


Figure 10.6. Float-zone process. (*a*) Schematic setup. (*b*) Simple model for doping evaluation.

Figure 10.8. Relative impurity concentration versus zone length for a number of passes. *L* denotes the zone length.[4]

Material Characterization – Wafer shaping

- Remove seed with diamond saw
- Grind exterior surface to establish desired diameter
- Grind “flats” along ingot
  - Planes (crystal orientation and doping type)
- **Primary flat** - used as mechanical locator for subsequent processing steps
- **Secondary flats** – identify orientation & conductivity type
- Slice wafer with diamond saw
  - Surface orientation [<111> & <100> common for Si]
  - Thickness [0.5 to 0.7 mm]
  - Taper – thickness variations across wafer
  - Bow – curvature variation from center to edge
- Mechanical lapping/polishing
  - Polish one or both sides of wafer
  - Lapped using mixture of Al_2O_3 & glycerine
  - Flatness uniformity within 2 µm

Wafer Identification

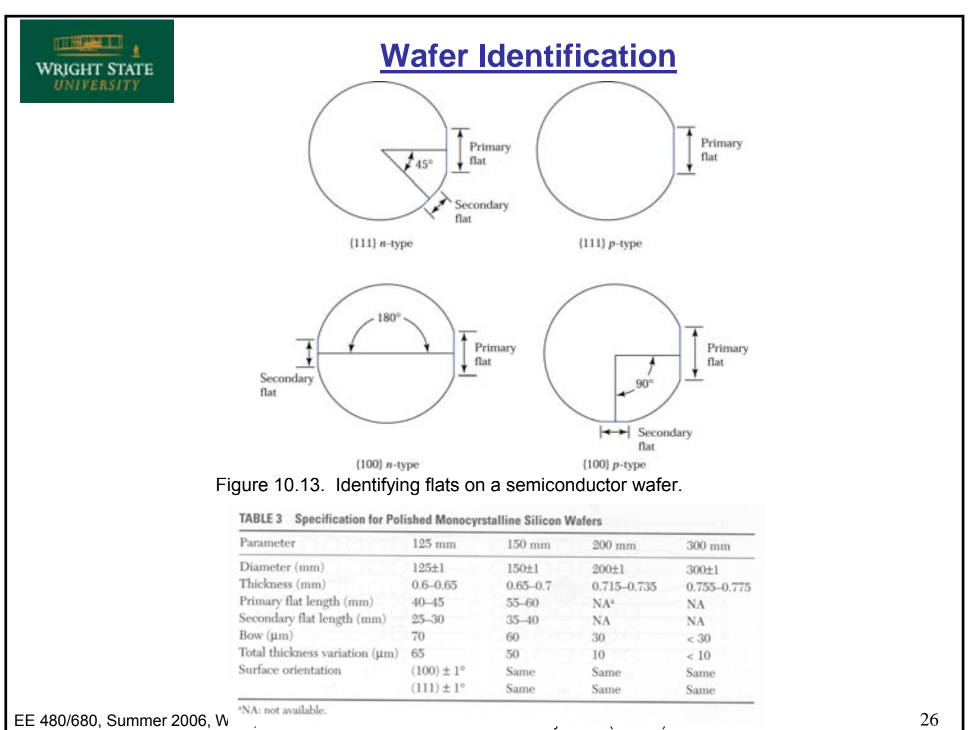


Figure 10.13. Identifying flats on a semiconductor wafer.

TABLE 3 Specification for Polished Monocyrstalline Silicon Wafers

Parameter	125 mm	150 mm	200 mm	300 mm
Diameter (mm)	125±1	150±1	200±1	300±1
Thickness (mm)	0.6–0.65	0.65–0.7	0.715–0.735	0.755–0.775
Primary flat length (mm)	40–45	55–60	NA[a]	NA
Secondary flat length (mm)	25–30	35–40	NA	NA
Bow (µm)	70	60	30	< 30
Total thickness variation (µm)	65	50	10	< 10
Surface orientation	(100) ± 1°	Same	Same	Same
	(111) ± 1°	Same	Same	Same

[a]NA: not available.

Crystal Characterization

- Real crystals are not perfect – they have defects –two types
- Localized
  - Point defect – any foreign atom incorporated into the lattice structure either a substitutional site or an interstitial site
  - Missing atoms (host atoms)
  - Frenkel defect – host atom is situated between regular lattice sites & adjacent to a vacancy
- Non-Localized
  - Line – an extra or incomplete plane results in an edge dislocation
  - Area
    - Twinning – change in the crystal orientation across a plane
    - Grain boundary – transition region between single-crystal regions within a polycrystalline material
  - Volume – impurities or dopants migrate to form a specific high concentration region
    - Precipitates of impurities cause dislocations because of atom size mismatch
- Some defects can be removed by high temperature anneals

Crystal Defects

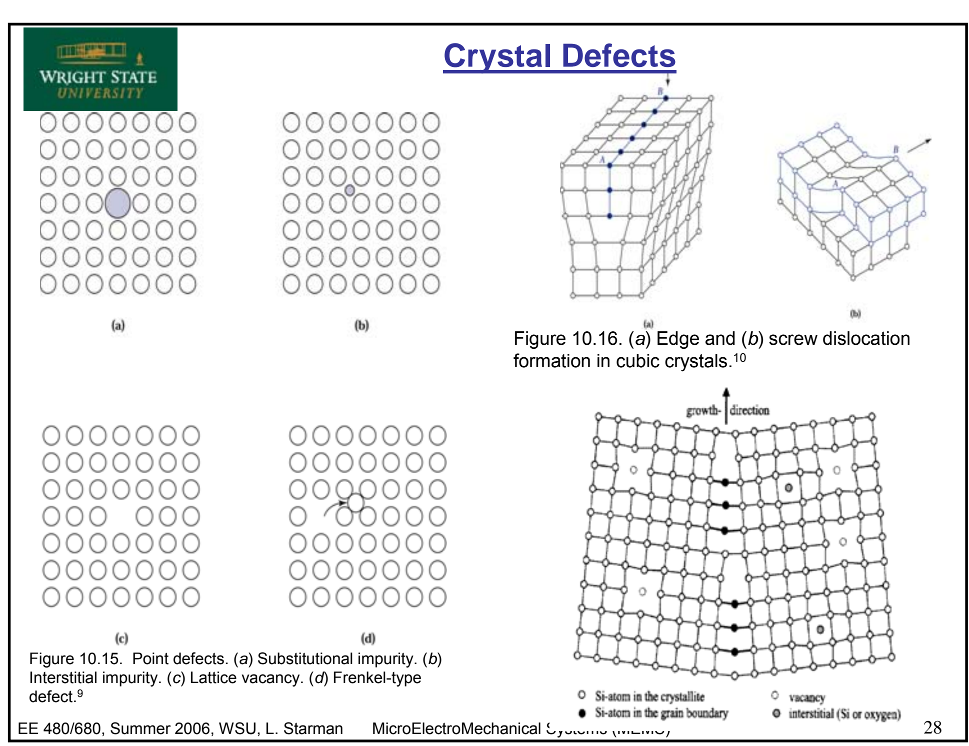
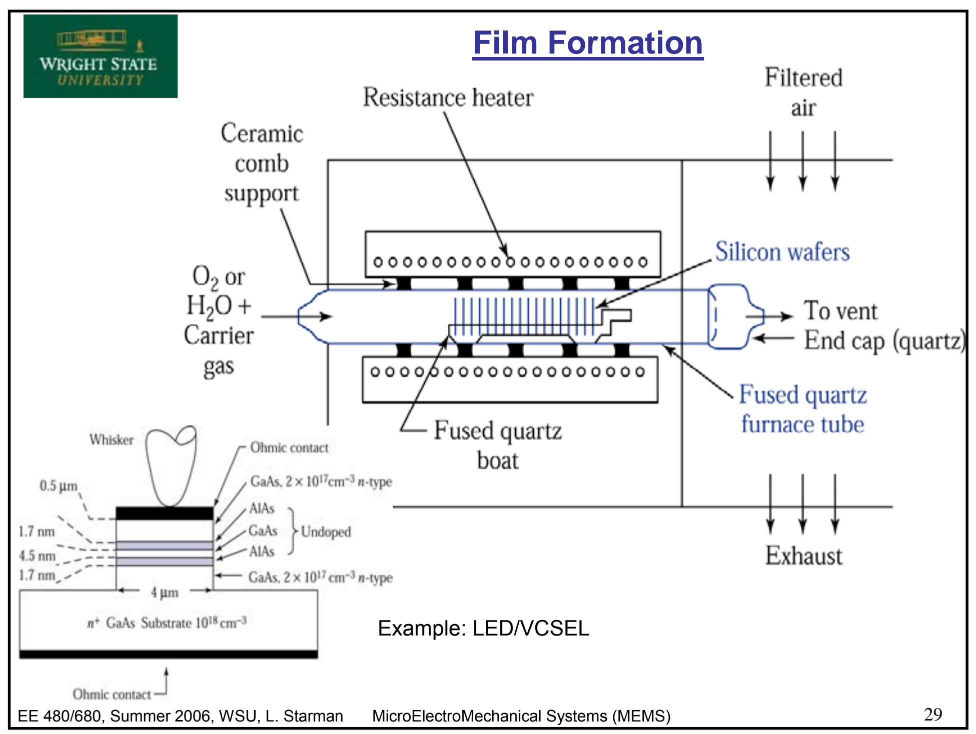


Figure 10.16. (*a*) Edge and (*b*) screw dislocation formation in cubic crystals.[10]

Figure 10.15. Point defects. (*a*) Substitutional impurity. (*b*) Interstitial impurity. (*c*) Lattice vacancy. (*d*) Frenkel-type defect.[9]

Film Formation



Example: LED/VCSEL

Epitaxy

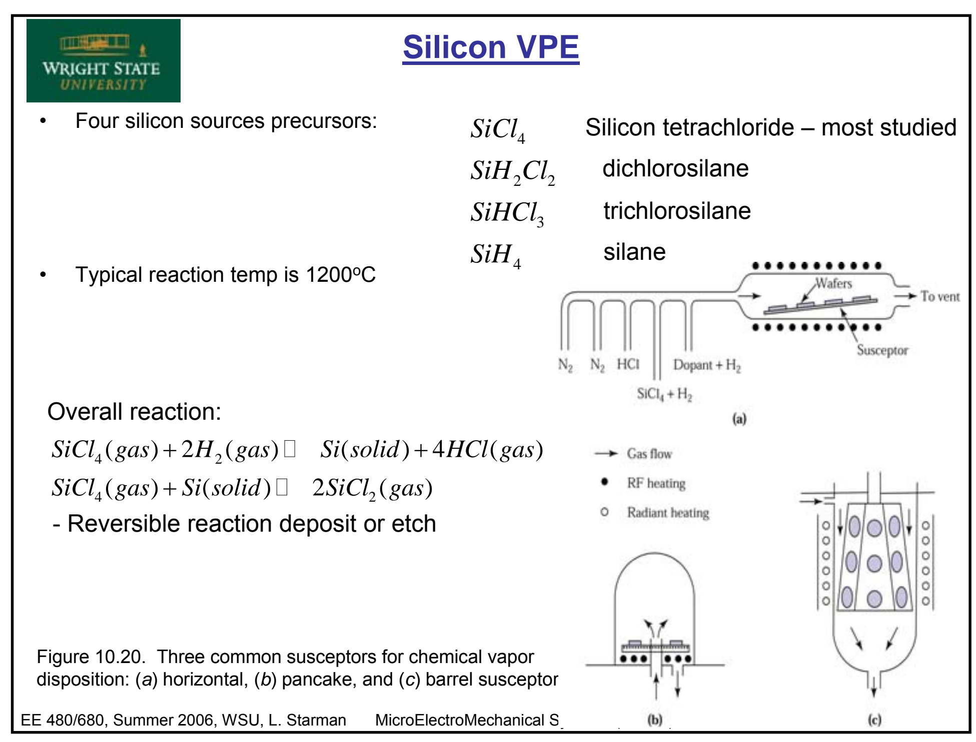
- Substrate wafer acts as the seed crystal
- The regular oriented growth of a single crystal layer(s) with controlled thickness and doping over a similar single crystal called the substrate
- Originally used to make high quality materials with characteristics superior to those of substrates
- Today, epitaxial techniques are used for the synthesis of ultra thin layers (monolayers), precise doping profiles or uniformity, and variable material compositions – in addition to low defect density material
- Enhances performance of devices and opens up many new possibilities
- Epitaxy processes occur at temps 30-50% lower than the melting pt.
- Types of epitaxial processes:
  - Vapor phase epitaxy (VPE) – metalorganic vapor phase epitaxy (MOVPE)
  - Liquid phase epitaxy (LPE) – rarely used
  - Molecular beam epitaxy (MBE) – MOMBE, gas source MBE (GSMBE), atomic layer epitaxy (ALE)

Vapor Phase Epitaxy (VPE)

- Also called CVD – chemical-vapor deposition
- Epi growth by vapor transport of reactants
- Precursors – are mixed with a "carrier gas" (i.e. H_2) which dilutes the mixer
- The gas, with its proportionate constituents, flows over or toward a heated substrate
- Some of the precursors are "cracked" into atom/molecule fragments while diffusing toward substrate surface (GaH_2 gas)
- At the surface, the atoms move to an appropriate lattice site and incorporate – else they recombine with other fragments
- Stagnant boundary layers form above the substrate from which reactant atoms/molecules diffuse to the substrate surface

VPE Advantages/Disadvantages

- **Advantages**
  - Low temperature process
  - High purity (low defect density) material
  - Readily automated for mass production
  - Ability to grow thin layers with precise composition, doping density, thickness O on an atomic scale for advanced systems)
  - Well suited to research – has opened "new" physics
- **Disadvantages**
  - Toxic gases are used – must have gas monitors and stainless steel plumbing. The exhaust pump system includes a 'scrubber' that breaks down toxic end products before atmospheric release (burn the gases)
  - Research systems are expensive, as are many of the precursors (purchased as pressurized gases in cylinders or as 'bubbler's'
- VPE works well with Si and GaAs (usually not used) – and related elemental and compound semiconductors



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Silicon VPE
• Four silicon sources precursors:
$SiCl_4$ Silicon tetrachloride – most studied
SiH_2Cl_2 dichlorosilane
$SiHCl_3$ trichlorosilane
SiH_4 silane
• Typical reaction temp is 1200ºC
Overall reaction:
$SiCl_4(gas) + 2H_2(gas) \leftrightarrow Si(solid) + 4HCl(gas)$
$SiCl_4(gas) + Si(solid) \leftrightarrow 2SiCl_2(gas)$
- Reversible reaction deposit or etch
Wafers
To vent
Susceptor
N2 N2 HCl Dopant + H2
SiCl4 + H2
(a)
Gas flow
RF heating
Radiant heating
(b)
(c)
Figure 10.20. Three common susceptors for chemical vapor disposition: (a) horizontal, (b) pancake, and (c) barrel susceptor
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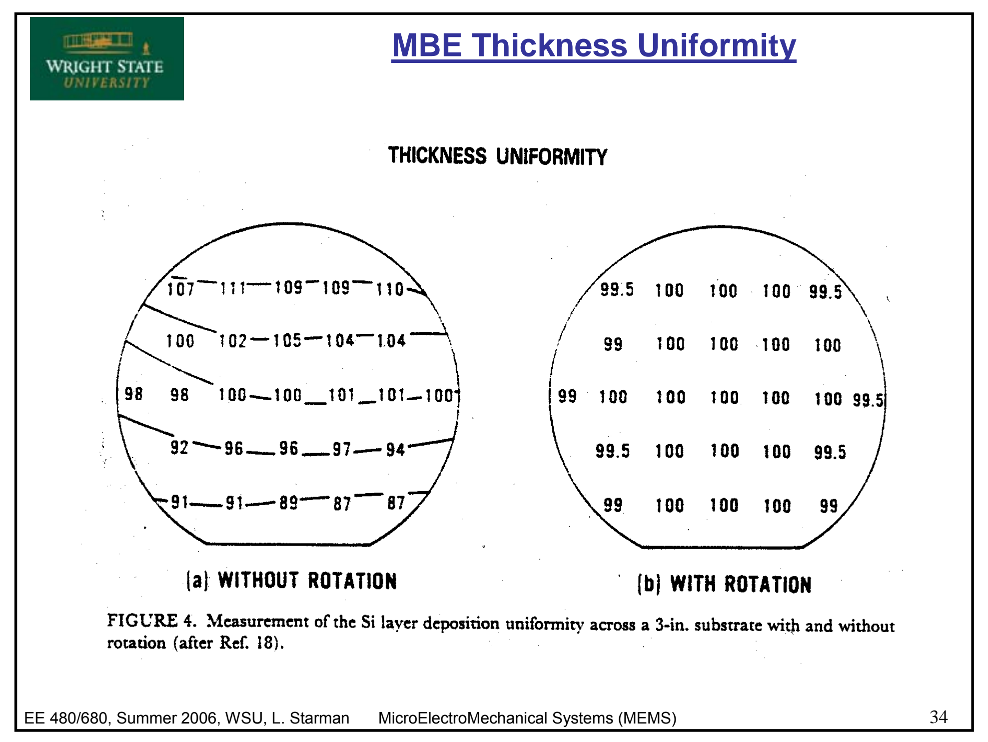

WRIGHT STATE UNIVERSITY
MBE Thickness Uniformity
THICKNESS UNIFORMITY
107 111 109 109 110
100 102 105 104 104
98 98 100 100 101 101 100
92 96 96 97 94
91 91 89 87 87
(a) WITHOUT ROTATION
99.5 100 100 100 99.5
99 100 100 100 100
99 100 100 100 100 100 99.5
99.5 100 100 100 99.5
99 100 100 100 99
(b) WITH ROTATION
FIGURE 4. Measurement of the Si layer deposition uniformity across a 3-in. substrate with and without rotation (after Ref. 18).
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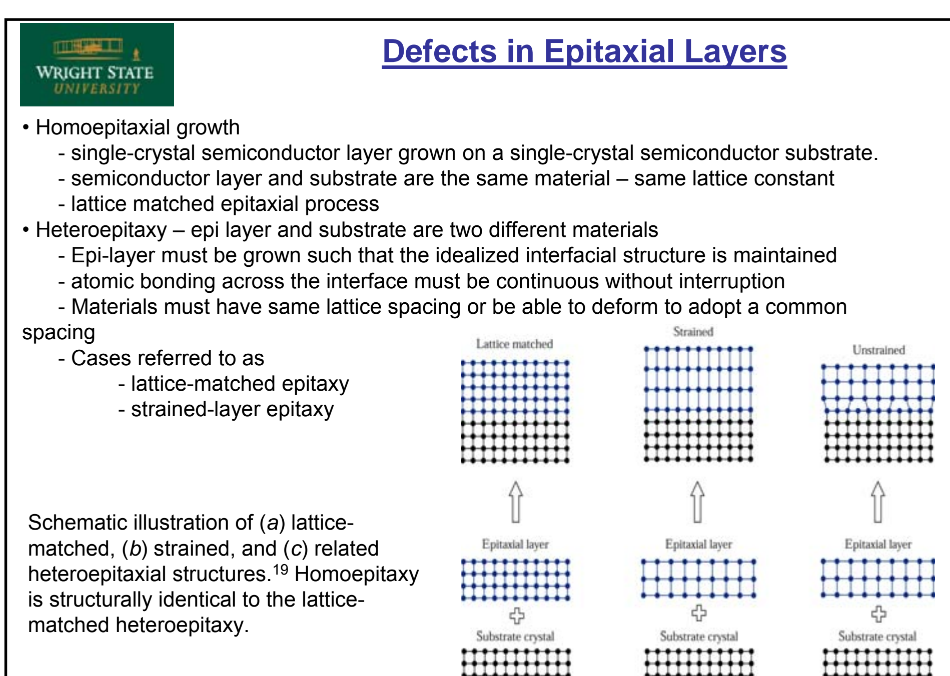
WRIGHT STATE UNIVERSITY
Defects in Epitaxial Layers
• Homoepitaxial growth
- single-crystal semiconductor layer grown on a single-crystal semiconductor substrate.
- semiconductor layer and substrate are the same material – same lattice constant
- lattice matched epitaxial process
• Heteroepitaxy – epi layer and substrate are two different materials
- Epi-layer must be grown such that the idealized interfacial structure is maintained
- atomic bonding across the interface must be continuous without interruption
- Materials must have same lattice spacing or be able to deform to adopt a common spacing
- Cases referred to as
- lattice-matched epitaxy
- strained-layer epitaxy
Lattice matched
Strained
Unstrained
Epitaxial layer
Epitaxial layer
Epitaxial layer
Substrate crystal
Substrate crystal
Substrate crystal
(a)
(b)
(c)
Schematic illustration of (a) lattice-matched, (b) strained, and (c) related heteroepitaxial structures.19 Homoepitaxy is structurally identical to the lattice-matched heteroepitaxy.
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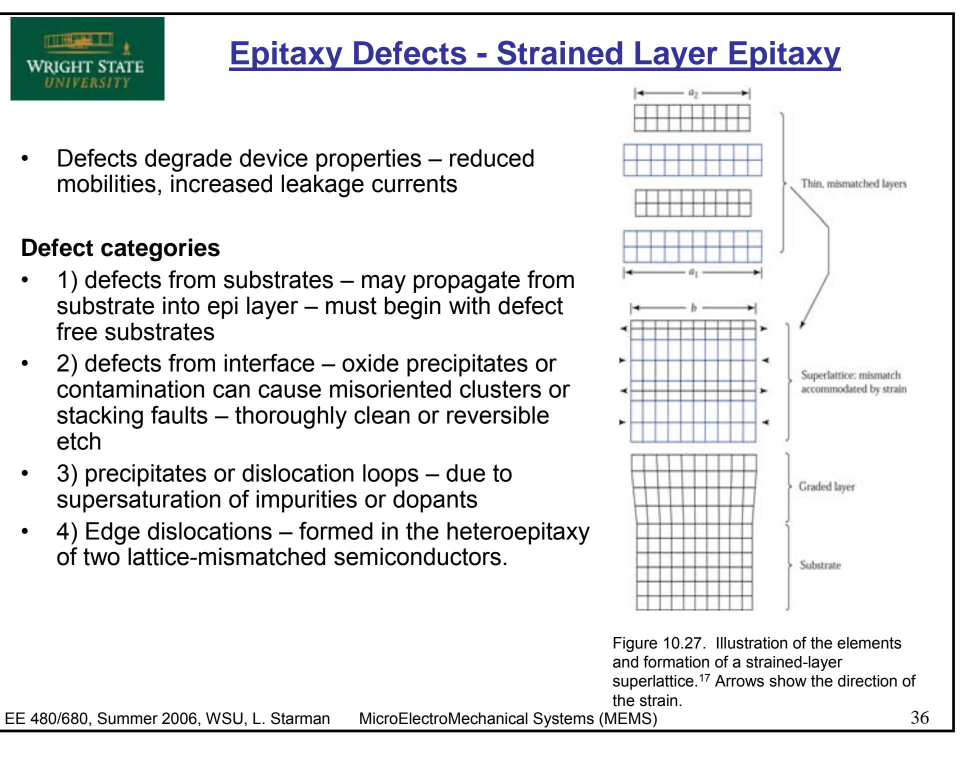
WRIGHT STATE UNIVERSITY
Epitaxy Defects - Strained Layer Epitaxy
• Defects degrade device properties – reduced mobilities, increased leakage currents
Defect categories
• 1) defects from substrates – may propagate from substrate into epi layer – must begin with defect free substrates
• 2) defects from interface – oxide precipitates or contamination can cause misoriented clusters or stacking faults – thoroughly clean or reversible etch
• 3) precipitates or dislocation loops – due to supersaturation of impurities or dopants
• 4) Edge dislocations – formed in the heteroepitaxy of two lattice-mismatched semiconductors.
a2
a1
b
Thin, mismatched layers
Superlattice: mismatch accommodated by strain
Graded layer
Substrate
Figure 10.27. Illustration of the elements and formation of a strained-layer superlattice.17 Arrows show the direction of the strain.
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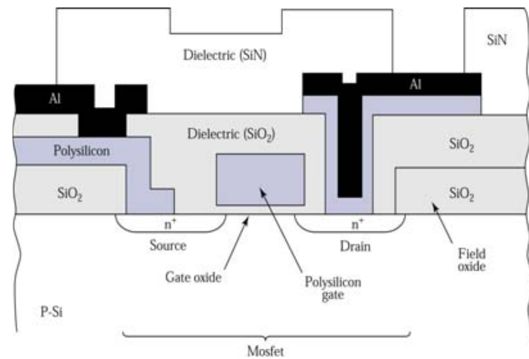
Oxidation & Film Deposition

- The creation of non-crystalline films used for non-semiconductor behavior
- current conduction or isolation
- IC fabrication requires many types of films
  - Thermal oxides – highest quality
  - Dielectric layers – lower quality
  - Polycrystalline films
  - Metal films



Schematic cross section of a metal-oxide-semiconductor field-effect transistor (MOSFET).

Oxidation & Deposition

- Thermal oxides
  - gate oxide (establish the source to drain conducting channel)
  - Wet oxidation results in rapid growth but the resultant oxide is very porous (gaps in the amorphous SiO_2 crystal)
  - Dry oxidation results in a slower growth rate but higher density & smaller defect (traps/interface states) density $SiO_2 \rightarrow$ best quality
- Field oxide
  - isolation of similar devices on the substrate. High quality oxides with low impurity densities are required to minimize leakage currents
  - Mask for diffusion/implants
  - Surface passivation (CVD)
- Dielectric layers
  - deposited SiO_2 and Si_3N_4
  - Used for insulation between conductors, as an ion implantation mask, or as passivation layer(s)
- Polycrystalline silicon (Poly)
  - serves as a gate electrode or a conductive material for multi-level metallizations
- Metal films
  - Al, silicides, Au for low resistance interconnects/bonding pads

General requirements

• be definable by lithography and etching

• Perform function and be compatible chemically and physically with the surface below, and any surface applied above

Growth Mechanism and Kinetics

Dry
-- Si (solid) + O_2 (gas) → SiO_2 (solid)
Wet/steam
-- Si (solid) + $2H_20$ (gas) → SiO_2 (solid) + $2H_2$ (gas)

- In order for the oxidizing species to reach the Si/SiO_2 interface and "grow" the oxide
  - species must be transported from the bulk of the gas to the oxide/gas interface
  - species must diffuse across (through) the oxide layer already present and get to the Si
  - then, the species chemically reacts at the Si interface to produce an oxide
- During the oxidation process, a portion of the Si wafer is consumed – and the resulting oxide expands upward during growth (relative to the original Si/air position)
- Si/SiO_2 interface moves into the silicon during the oxidation process.
- Densities & molecular weights of Si & SiO_2 used to show that growing an oxide of thickness *x* consumes a layer of silicon 0.44*x* thick

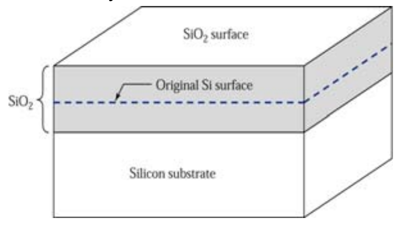


Figure 11.3. Growth of silicon dioxide by thermal oxidation.

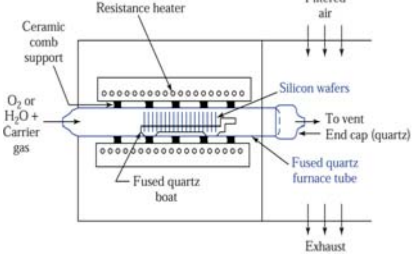


Figure 11.2. Schematic cross section of a resistance-heated oxidation furnace.

Simple model/growth model:

Volume of one mole:

Molecular weight of Si/Density of Si → $Si = \frac{M_{si}}{\rho_{si}} = \frac{28.09(g/mole)}{2.33(g/cm^3)} = 12.06(cm^3/mole)$

Molecular weight of SiO_2/Density of SiO_2 → $SiO_2 = \frac{60.08(g/mole)}{2.21(g/cm^3)} = 27.18(cm^3/mole)$

Thickness of Si x Area/Thickness of SiO_2 x Area = Volume of 1 mol of Si/volume of 1 mol of SiO_2

$$\frac{Vol(Si)}{Vol(SiO_2)} = \frac{12.06(cm^3/mole)}{27.18(cm^3/mole)} = 0.44$$

Equation Format: $N_s(AX_s) = N_{ox}(AX_{ox})$

$N_s \equiv$ Density of silicon

$A \equiv$ Area

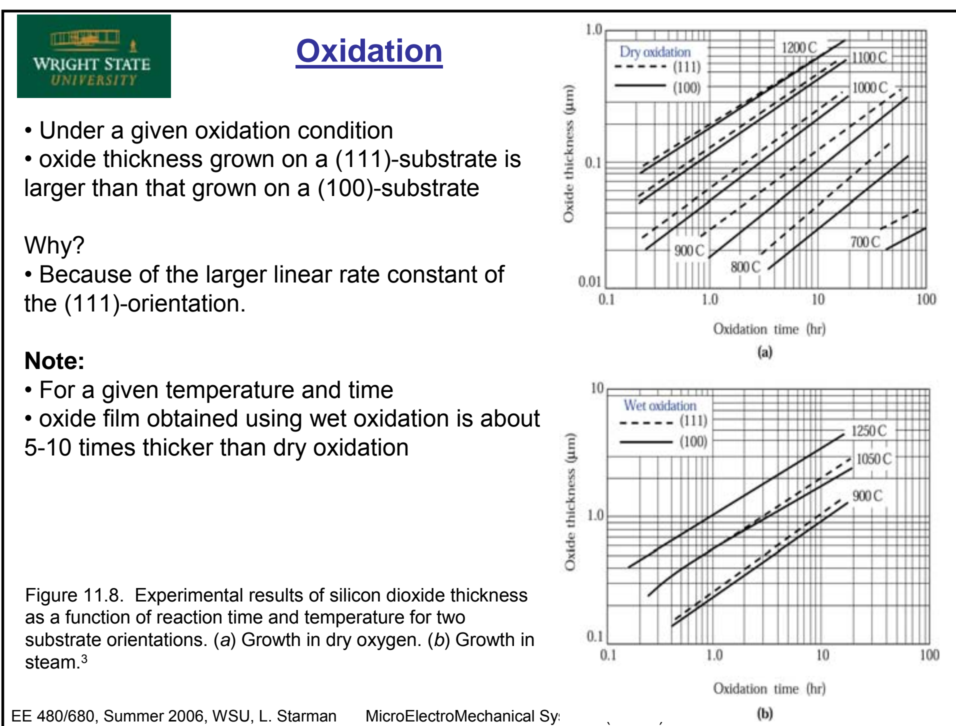
$X_s \equiv$ thickness of silicon consumed

$N_{ox} \equiv$ Density of the oxide

$X_{ox} \equiv$ thickness of the oxide layer

$$X_s = \frac{N_{ox}X_{ox}}{N_s} = 0.44X_{ox}$$

- Utility – thin oxides (≤ 1000 Ang) use dry process (perform electrical device functions)
  thick oxides (≥ 5000 Ang) use wet process – faster growth, lower quality, used for isolation


WRIGHT STATE UNIVERSITY
Oxidation
• Under a given oxidation condition
• oxide thickness grown on a (111)-substrate is larger than that grown on a (100)-substrate
Why?
• Because of the larger linear rate constant of the (111)-orientation.
Note:
• For a given temperature and time
• oxide film obtained using wet oxidation is about 5-10 times thicker than dry oxidation
Figure 11.8. Experimental results of silicon dioxide thickness as a function of reaction time and temperature for two substrate orientations. (a) Growth in dry oxygen. (b) Growth in steam.3
Dry oxidation
(111)
(100)
1200 C
1100 C
1000 C
900 C
800 C
700 C
Oxide thickness (μm)
Oxidation time (hr)
(a)
Wet oxidation
(111)
(100)
1250 C
1050 C
900 C
Oxide thickness (μm)
Oxidation time (hr)
(b)
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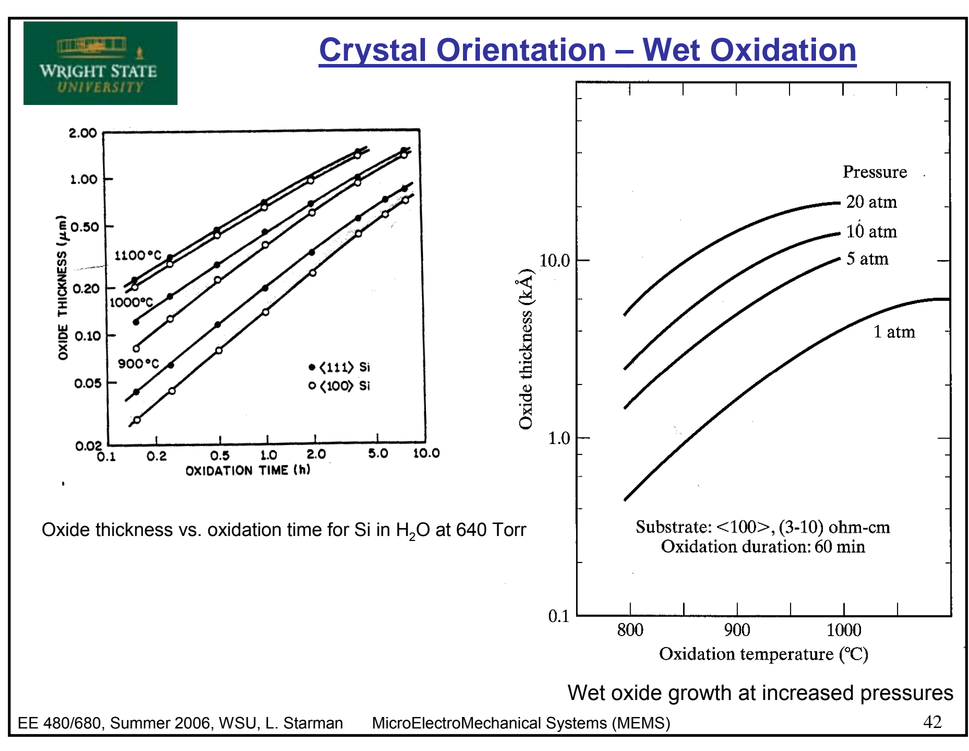
WRIGHT STATE UNIVERSITY
Crystal Orientation – Wet Oxidation
OXIDE THICKNESS (μm)
OXIDATION TIME (h)
1100°C
1000°C
900°C
● ⟨111⟩ Si
○ ⟨100⟩ Si
Oxide thickness vs. oxidation time for Si in H2O at 640 Torr
Pressure
20 atm
10 atm
5 atm
1 atm
Oxide thickness (kÅ)
Substrate: <100>, (3-10) ohm-cm
Oxidation duration: 60 min
Oxidation temperature (℃)
Wet oxide growth at increased pressures
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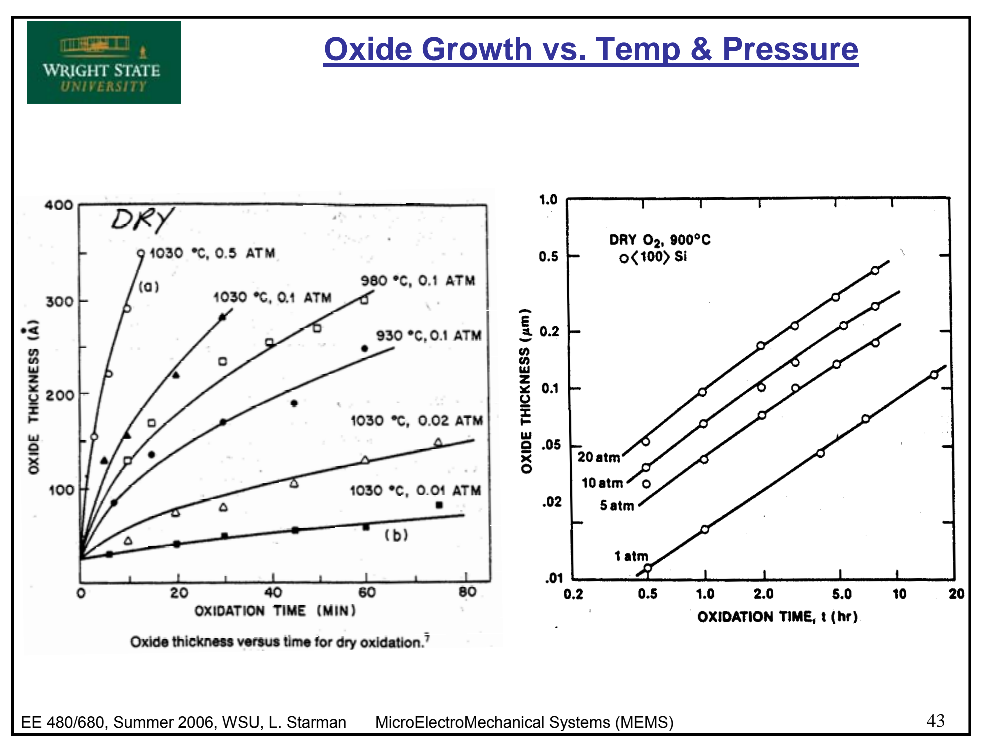
Oxide Growth vs. Temp & Pressure
WRIGHT STATE UNIVERSITY
DRY
1030 °C, 0.5 ATM
1030 °C, 0.1 ATM
980 °C, 0.1 ATM
930 °C, 0.1 ATM
1030 °C, 0.02 ATM
1030 °C, 0.01 ATM
OXIDE THICKNESS (Å)
OXIDATION TIME (MIN)
Oxide thickness versus time for dry oxidation.
DRY O2, 900°C
<100> Si
20 atm
10 atm
5 atm
1 atm
OXIDE THICKNESS (μm)
OXIDATION TIME, t (hr)
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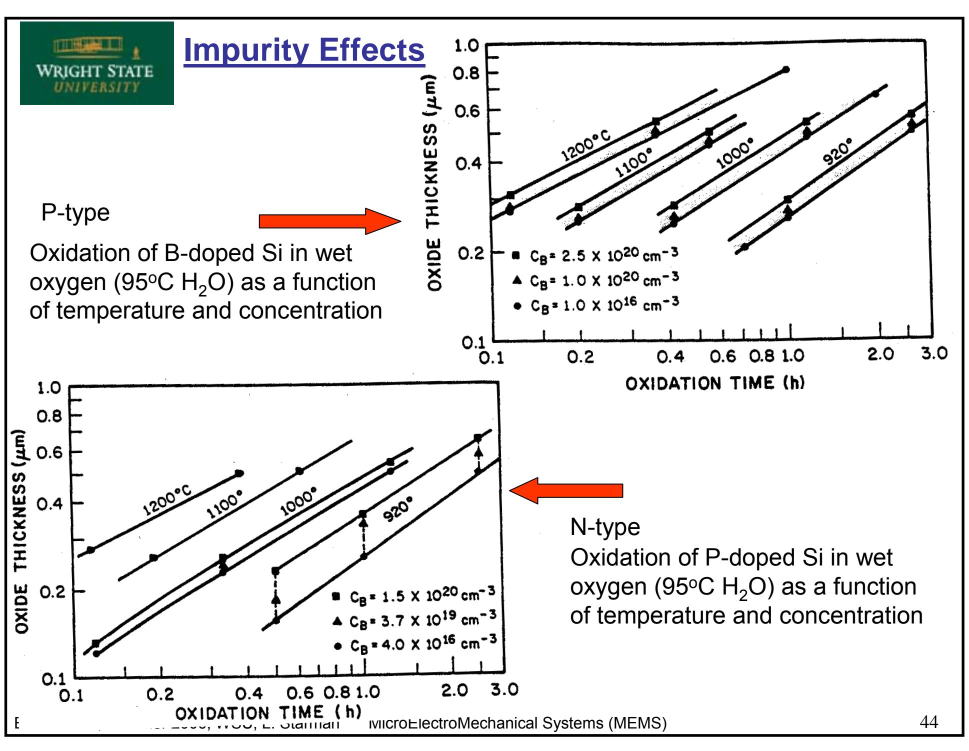
Impurity Effects
WRIGHT STATE UNIVERSITY
P-type
Oxidation of B-doped Si in wet oxygen (95oC H2O) as a function of temperature and concentration
1200°C
1100°
1000°
920°
CB = 2.5 X 10^20 cm^-3
CB = 1.0 X 10^20 cm^-3
CB = 1.0 X 10^16 cm^-3
OXIDE THICKNESS (μm)
OXIDATION TIME (h)
N-type
Oxidation of P-doped Si in wet oxygen (95oC H2O) as a function of temperature and concentration
CB = 1.5 X 10^20 cm^-3
CB = 3.7 X 10^19 cm^-3
CB = 4.0 X 10^16 cm^-3
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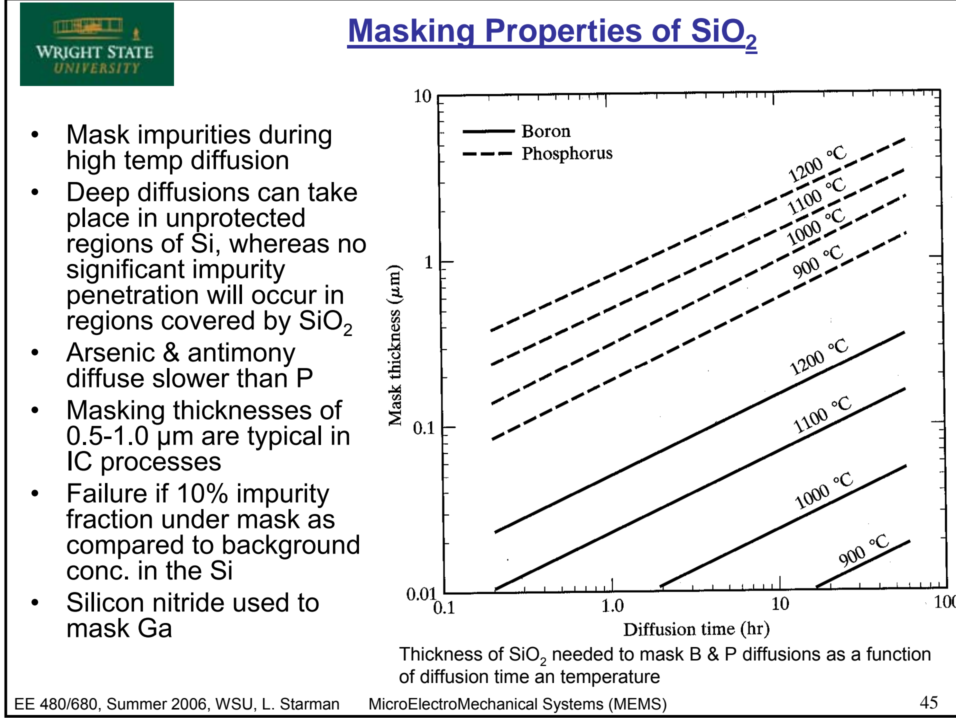
WRIGHT STATE UNIVERSITY
Masking Properties of SiO2
Mask impurities during high temp diffusion
Deep diffusions can take place in unprotected regions of Si, whereas no significant impurity penetration will occur in regions covered by SiO2
Arsenic & antimony diffuse slower than P
Masking thicknesses of 0.5-1.0 µm are typical in IC processes
Failure if 10% impurity fraction under mask as compared to background conc. in the Si
Silicon nitride used to mask Ga
Boron
Phosphorus
1200 °C
1100 °C
1000 °C
900 °C
Mask thickness (µm)
Diffusion time (hr)
Thickness of SiO2 needed to mask B & P diffusions as a function of diffusion time an temperature
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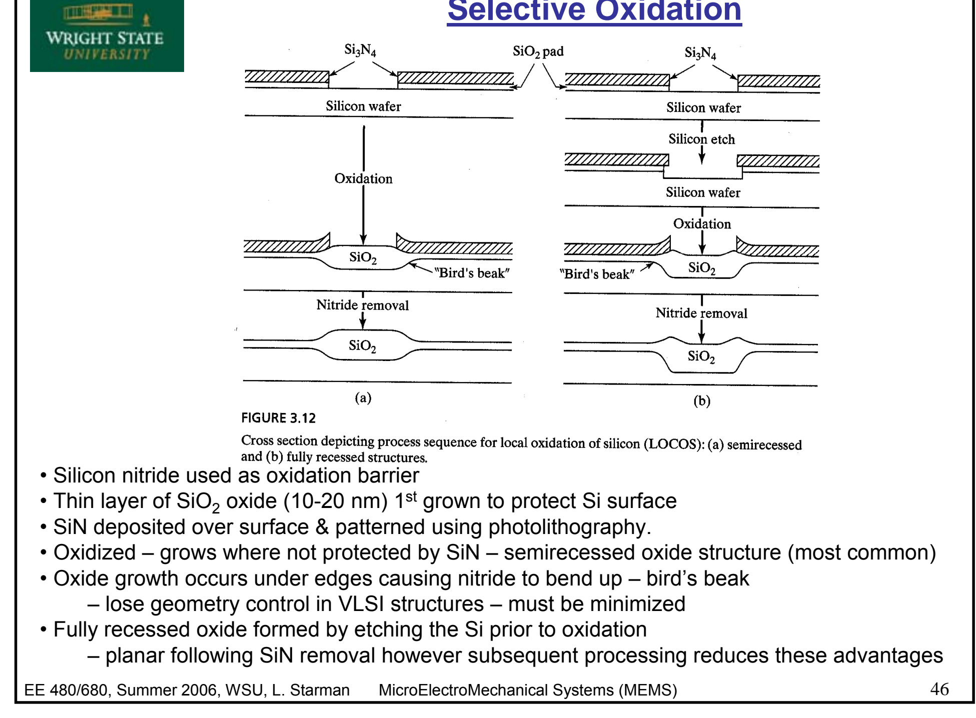
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Selective Oxidation
Si3N4
SiO2 pad
Silicon wafer
Silicon etch
Oxidation
SiO2
"Bird's beak"
Nitride removal
(a)
(b)
FIGURE 3.12
Cross section depicting process sequence for local oxidation of silicon (LOCOS): (a) semirecessed and (b) fully recessed structures.
Silicon nitride used as oxidation barrier
Thin layer of SiO2 oxide (10-20 nm) 1st grown to protect Si surface
SiN deposited over surface & patterned using photolithography.
Oxidized – grows where not protected by SiN – semirecessed oxide structure (most common)
Oxide growth occurs under edges causing nitride to bend up – bird's beak
– lose geometry control in VLSI structures – must be minimized
Fully recessed oxide formed by etching the Si prior to oxidation
– planar following SiN removal however subsequent processing reduces these advantages
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Dielectric & Polysilicon Deposition

- Widely used in modern VLSI circuits
- Provide conducting regions, electrical insulation between metals, environmental protection
- Require uniform thickness & reproducible
- Most widely used material for film deposition (excluding metals)
  - Polycrystalline silicon – typically dope heavily n- or p-type
  - Silicon dioxide
  - Stoichiometric silicon nitride (Si_3N_4)
  - Plasma deposited silicon nitride
- Common deposition methods
  - Chemical vapor deposition (CVD)
  - Low pressure chemical vapor deposition (LPCVD)
  - Plasma enhanced chemical vapor deposition (PECVD)

Polycrystalline Si (Poly or polysilicon)

PolySi

- Pyrolize silane (SiH_4) at 575-650°C (break apart silane)
- Conducting lines for multilevel metallization
- Contact for shallow junctions
- Usually deposited without dopants (but not always)
- Dopants (As, P, B) reduce ρ (resistivity) - added by diffusion or ion implantation

Silicon dioxide (CVD films)

- Dielectric insulator between conducting films
- Masks for diffusion and ion implantation
- Diffusion source – from doped oxides
- Capping doped films/Si – prevent dopant loss
- Gettering impurities – process which removes harmful impurities or defects
- Phosphorous-doped SiO_2 (P-glass) used as doping source
  - i.e. phosphosilicate glass or PSG
  - Inhibits diffusion of Na, softens & flows at 950-1100°C – creating a smooth topography →good for subsequent metal, enhances hydrophobicity
- Borophosphosilicate glass (BPSG) – flows at 850-950°C – over wafer surface like PR

Silicon Nitride

- Nearly impervious to moisture
- Si_3N_4 deposited at 700-900°C is used as an oxidation mask
- Plasma deposited silicon nitride (SiNH) forms at 200-350°C – used for passivation. The low T allows for deposition over Au or Al

CVD Techniques (most often used for deposition)

- Temp range 100-1000°C
- Pressure range 0.05 Torr – 760 Torr (1 atm)
- Reaction energy → supplied by photons, glow discharge, thermal
- Poly & dielectric films have historically been deposited at 1 atm in a variety of reactor geometries
- Wafer(s) are placed on susceptor(s) heated by radiation using high intensity lamps, RF induction, or electrical resistance
- Horizontal reactors flow gas across the hot wafers, often at high velocity
- Vertical reactors often consist of a bell jar chamber with samples on a rotating assemble, perpendicular to gas flow

Plasma CVD

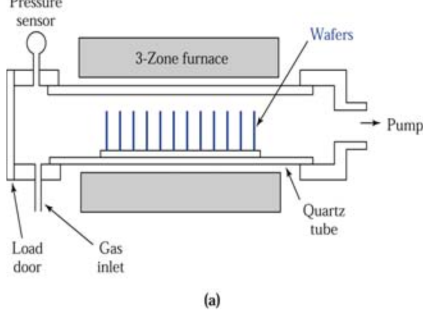
Plasma CVD

- Cylindrical reaction chamber made of quartz or stainless steel (with a view port)
- Capacitor (parallel plate) electrodes made of Al
- Samples lay on the bottom Al capacitor plate (or on a quartz plate placed on the Al plate)
- System is heated resistively (100-400°C)
- The source gas flows radially throughout the reaction chamber
- Used for SiO_2 & Si_3N_4
- Advantages
  - Low temperatures
  - Fast, easy
- Disadvantages
  - Limited capacity
  - Manual load/unload, gas purge, etc
  - Wafer contamination

CVD Reactors

Considerations in selecting a deposition process

- Substrate temperature
- Deposition rate
- Film uniformity
- Morphology
- Electrical properties
- Mechanical properties
- Chemical composition of dielectric films



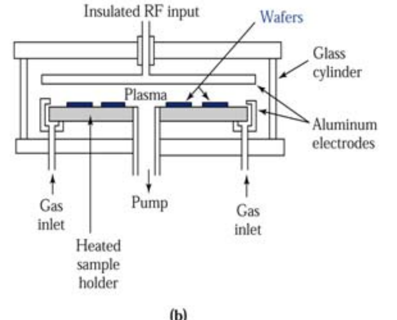


Figure 11.9. Schematic diagrams of chemical-vapor deposition reactors. (*a*) Hot-wall, reduced-pressure reactor. (*b*) Parallel-plate plasma deposition reactor.[4] rf, radio frequency.

Silicon Dioxide

TABLE 1 Properties of SiO_2 Films

Property	Thermally grown at 1000°C	$SiH_4 + O_2$ at 450°C	TEOS at 700°C	$SiCl_2H_2 + N_2O$ at 900°C
Composition	SiO_2	SiO_2 (H)	SiO_2	SiO_2(Cl)
Density (g/cm^3)	2.2	2.1	2.2	2.2
Refractive index	1.46	1.44	1.46	1.46
Dielectric strength (10^6 V/cm)	>10	8	10	10
Etch rate (Å /min) (100:1 H_2O:HF)	30	60	30	30
Etch rate (Å /min) (buffered HF)	440	1200	450	450
Step coverage	—	Nonconformal	Conformal	Conformal

- Deposition methods
- For **low-temp** deposition (300-500°C)

$$SiH_4 + O_2 \xrightarrow{450^o C} SiO_2 + 2H_2$$

$$4PH_3 + 5O_2 \xrightarrow{450^o C} 2P_2O_5 + 6H_2$$

- For **intermediate-temp** deposition (500-800°C)

$$\underbrace{Si(OC_2H_5)_4}_{} \xrightarrow{700^o C} SiO_2 + by-products$$

Tetraethylorthosilicate (TEOS)

- Suitable for Polysilicon gates requiring a uniform insulating layer with good step coverage.

- For **High-temp** deposition (900°C)

$$SiCl_2H_2 + 2N_2O \xrightarrow{900^o C} SiO_2 + 2N_2 + 2HCl$$

- Deposition gives excellent film uniformity & sometimes used to deposit insulating layers over polysilicon

NOTE: CVD SiO_2 does not replace thermally grown oxides as best electrical properties are obtained from thermally grown films

Polysilicon Deposition

- Pyrolyze silane at 575-650°C in a low pressure reactor

$$SiH_4 \rightarrow Si + 2H_2$$

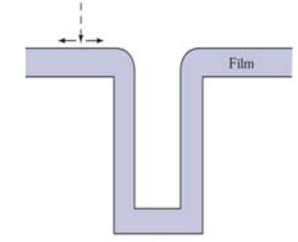
- Two common low pressure deposition recipes
  - 100% silane at 25-130 Pa (0.2-1.0 Torr)
  - 20-30% silane in N_2 at 25-130 Pa
  - Deposition rates are 10-20 nm/min
- Deposition of polysilicon depends on temp, pressure, silane concentration, and dopant concentration
- Polysilicon may be oxidized
- Usually done in dry O_2, T=900-1000°C
- Polysilicon properties
  - Density = 2.3 g/cm^3
  - Coefficient of thermal expansion - α = 2E-6/°C
  - Temp. coefficient of resistance – k = 1E-3/°C
- Addition of oxygen to polysilicon increases the film resistivity

$$SiH_4 \rightarrow Si + 2H_2$$

$$SiH_4 + xN_2O \rightarrow SiO_x + 2H_2 + xN_2$$

Step Coverage

Conformal - Uniformity of the film thickness, regardless of topography, is due to the rapid migration of reactants after adsorption on the step surfaces

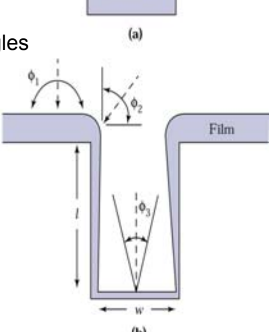


Non-conformal step coverage

$0 \leq \theta_1 \leq 180^o$ Top surface reactants come from many different angles

$0 \leq \theta_2 \leq 90^o$ Reactants arriving at the top of vertical wall

$\theta_3 \cong \tan^{-1}(\frac{W}{l})$ Related to width of opening and distance from top



- Film thickness on the top surface is double that of a wall surface
- This type of step coverage is thin along the vertical walls, with a possible crack at the bottom of step caused by self-shadowing
- Most evaporated (or sputtered) materials have a nonconformal step coverage

Figure 11.12. Step coverage of deposited films.
(*a*) Conformal step coverage.
(*b*) Nonconformal step coverage.[4]

Silicon Nitride CVD

$3SiH_4 + 4NH_3 \xrightarrow{700-800^o C(1Atm)} Si_3N_4 + 12H_2$ silane + ammonia

$3SiCl_2H_2 + 4NH_3 \xrightarrow{700-800^o C(<1Atm)} Si_3N_4 + 6HCl + 6H_2$ dichlorosilane + ammonia

Good film uniformity and high wafer throughput
Refractive index → related to composition

Properties of silicon nitride

Deposition	LPCVD	Plasma
Temperature (°C)	700–800	250–350
Composition	Si_3N_4(H)	SiN_xH_y
Si/N ratio	0.75	0.8–1.2
Atom % H	4–8	20–25
Refractive index	2.01	1.8–2.5
Density (g/cm^3)	2.9–3.1	2.4–2.8
Dielectric constant	6–7	6–9
Resistivity (ohm-cm)	10^{16}	10^6–10^{15}
Dielectric strength (10^6V/cm)	10	5
Energy gap (eV)	5	4–5
Stress (10^9 dyne/cm^2)	10 T	2C–5 T

SiN Plasma CVD

- **Si_3N_4**
- High tensile stress ~ 1E10 dyne/cm^2
- 1 Pa = 1N/m^2 = 1E-5 bar = 10 dyne/cm^2 = 7.501E-3 torr
- Films d > 200 nm sometimes crack due to the high stress

SiN Plasma CVD (usually radial flow, parallel plate, hot wall reactor)

$SiH_4 + NH_3 \rightarrow SiNH + 3H_2$ Argon plasma

$2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2$ Reduce silane in a nitrogen discharge

The products depend strongly on the deposition conditions
• Plasma deposited films contain large H concentrations

Other materials
• Silicon oxynitride (SiON)
• Al oxide, Al nitride, Ti oxide high ρ, ε
• Polyimides – spin and cure (300-350°C) → planar surfaces, poor thermal stability and moisture protection

Deposition Comparisons

Comparison of different deposition methods

	Atmospheric pressure CVD	Low temperature LPCVD	Medium temperature LPCVD	Plasma assisted CVD
Temperature (°C)	300 – 500	300 – 500	500 – 900	100 – 350
Materials	SiO_2 P-glass	SiO_2 P-glass BP-glass	Poly-Si SiO_2 P-glass BP-glass Si_3N_4 SiON SIPOS	SiNH SiO_2 SiON
Uses	Passivation, insulation	Passivation, insulation	Gate metal, insulation	Passivation, insulation
Throughput	High	High	High	Low
Step coverage	Poor	Poor	Conformal	Poor
Particles	Many	Few	Few	Many
Film properties	Good	Good	Excellent	Poor
Low temperature	Yes	Yes	No	Yes

Metallization

- Desired properties of the metallization for ICs, MEMS, & microelectronics
- Low resistivity
- Easy to form
- Easy to etch for pattern generation
- Should be stable in oxidizing ambients
- Mechanical stability; good adherence, low stress
- Surface smoothness
- Stability throughout processing, including high temp sinter, dry or wet oxidation, gettering, phosphorus glass (or any other material) passivation, metallization
- No reaction with final metal, aluminum
- Should not contaminate devices, wafers, or working apparatus
- Good device characteristics and lifetimes
- For window contacts – low contact resistance, minimal junction penetration, low electromigration
- Silicide – interface formed between Si & metal

Physical Vapor Deposition

- Most common methods
  - Evaporation – source material heated above melting point in evacuated chamber, evaporated atoms travel at high velocity in straight line trajectories. Heated by resistive, RF, or focus electron beam
  - E-beam evaporation
  - Plasma spray deposition
  - Sputtering – a source of ions is accelerated toward the target and impinged on its surface.
- Ti, Al, Cu, TiN, Au can be deposited this way

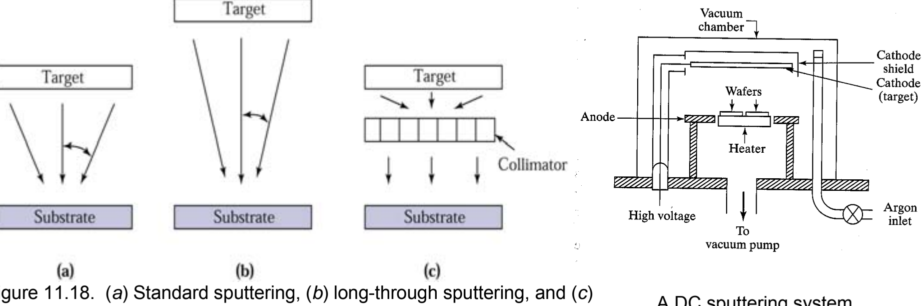
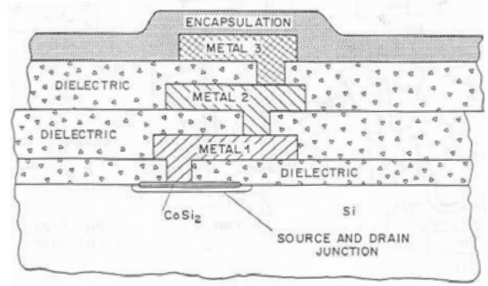


Figure 11.18. (*a*) Standard sputtering, (*b*) long-through sputtering, and (*c*) sputtering with a collimator.

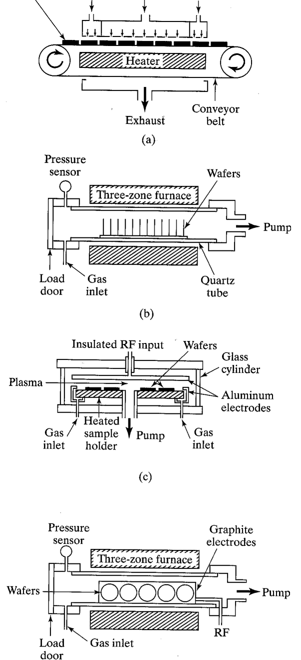
A DC sputtering system

Metal CVD Deposition

- CVD metallization offers
  - Conformal coating
  - Good step coverage
  - Coat a large # of wafers simultaneously
- Basic CVD setup is the same as the deposition of dielectrics and polysilicon



A schematic drawing of a multilevel metallization structure



Four types of CVD systems (a) APCVD, (b) hot-wall LPCVD using three zone furnace tube, (c) Parallel-polate plasma-enhanced, (d) PECVD

CVD of Metals

- Process by which a metal film is deposited by a chemical reaction or pyrolytic decomposition in the gas phase, in the neighborhood of the substrate
- Advantages
  - Conformal metal films (good step coverage)
  - Large # of wafers/run
  - Lower resistivity than with physical evaporation
  - Refractory metals
  - Useful for depositing heavy metals (i.e. W)

Chemistry (Tungsten) W

$$WF_6 \xrightarrow{pyrolysis} W + 3F_2$$

$$WF_6 + 3H_2 \xrightarrow[600-900oC]{reduction} W + 6HF$$ HF – very toxic, will “eat” your car’s windows

Other metals – Mo, Ta, Ti can be deposited by hydrogen reduction in an LPCVD reactor

$$2MCl_5 + 5H_2 \xrightarrow{600-800^o C} 2M + 10HCl$$

Al deposition using an MO source – tri-isobutyl aluminum (MO = metalorganic)

$$2[(CH_3)_2CHCH_2]_3Al \rightarrow 2Al + 3H_2 + by - products$$

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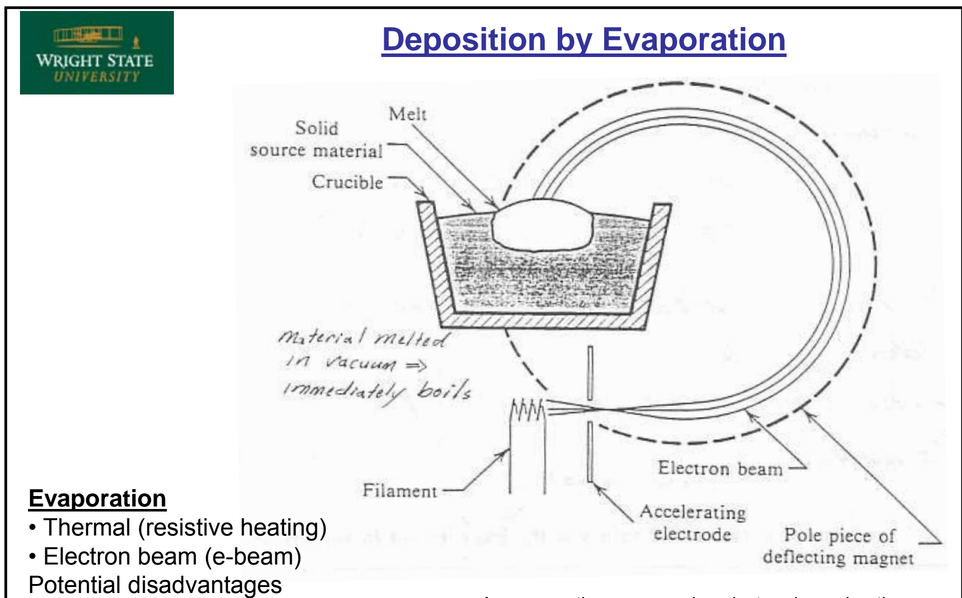
Deposition by Evaporation



An evaporation source using electron-beam heating. The beam is generated out of the line of sight of the source and is focused into it by a B-field. A heated filament supplies electrons, and the accelerating electrodes form them into a beam.

Evaporation
- Thermal (resistive heating)
- Electron beam (e-beam)

Potential disadvantages
- Source filament/crucible contamination
- Ionizing x-rays penetrate substrate, damage lattice

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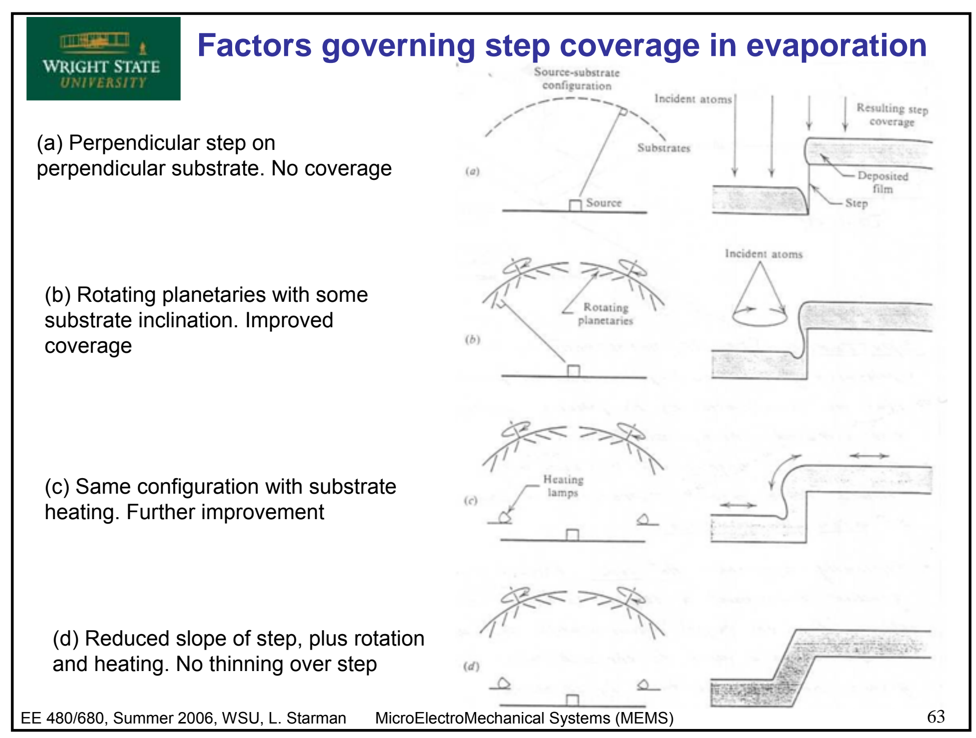
Factors governing step coverage in evaporation
(a) Perpendicular step on perpendicular substrate. No coverage
(b) Rotating planetaries with some substrate inclination. Improved coverage
(c) Same configuration with substrate heating. Further improvement
(d) Reduced slope of step, plus rotation and heating. No thinning over step
Source-substrate configuration
Incident atoms
Resulting step coverage
Substrates
Deposited film
Step
Source
Rotating planetaries
Heating lamps
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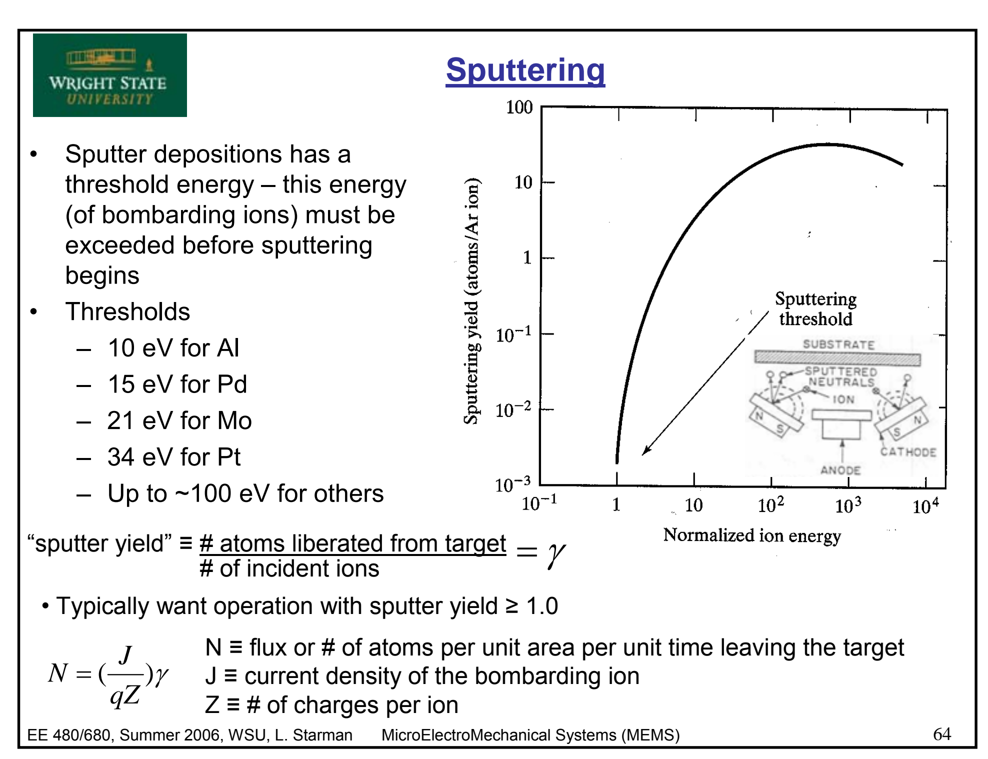
Sputtering
Sputter depositions has a threshold energy – this energy (of bombarding ions) must be exceeded before sputtering begins
Thresholds
– 10 eV for Al
– 15 eV for Pd
– 21 eV for Mo
– 34 eV for Pt
– Up to ~100 eV for others
Sputtering yield (atoms/Ar ion)
Normalized ion energy
Sputtering threshold
SUBSTRATE
SPUTTERED NEUTRALS
ION
CATHODE
ANODE
"sputter yield" ≡ # atoms liberated from target / # of incident ions = γ
• Typically want operation with sputter yield ≥ 1.0
N = (J/qZ)γ
N ≡ flux or # of atoms per unit area per unit time leaving the target
J ≡ current density of the bombarding ion
Z ≡ # of charges per ion
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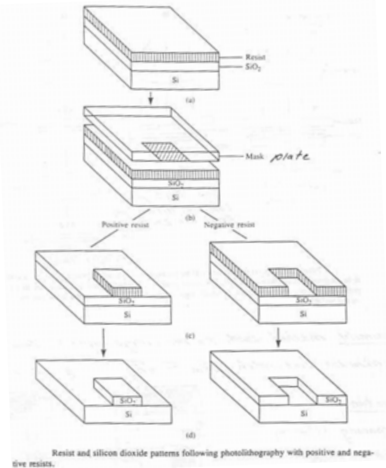
Lithography

- Transfer geometric patterns on a mask to a thin layer of radiation sensitive material (called resist) covering the surface of a semiconductor wafer
- Transfer stored geometric patterns (in a computer memory) to a thin resist layer as above (direct write)
  - Optical lithography
  - Electron beam lithography
  - X-ray lithography
  - Ion Beam lithography
- Optical lithography
  - ultraviolet radiation
  - (λ~ 0.2 to 0.4 μm)
  - resist ⇒ photoresist

Exposure Tool performance (3 parameters)

- Resolution – minimum feature dimension that can be transferred with high fidelity to a resist film
- Registration – measure of how accurately patterns on successive masks can be aligned
- Throughput – number of wafers that can be exposed per hour for a given mask level



Resist and silicon dioxide patterns following photolithography with positive and negative resists.

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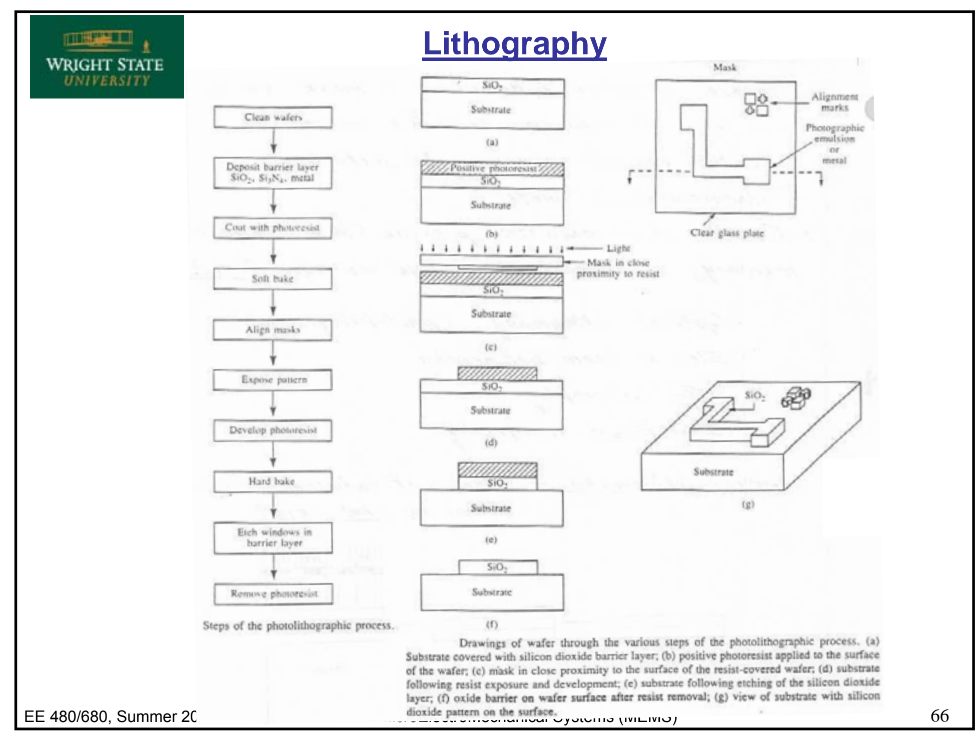
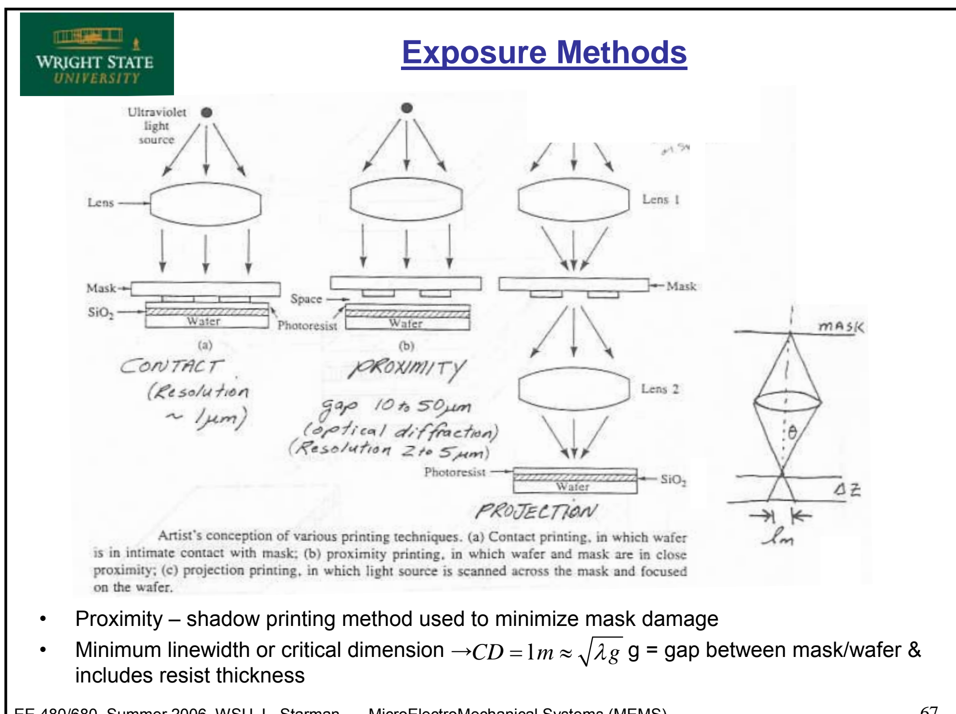
Lithography



Steps of the photolithographic process.

Drawings of wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.


Exposure Methods
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Ultraviolet light source
Lens
Mask
SiO2
Wafer
Space
Photoresist
Lens 1
Lens 2
(a)
(b)
CONTACT
(Resolution ~ 1μm)
PROXIMITY
gap 10 to 50μm
(optical diffraction)
(Resolution 2 to 5μm)
PROJECTION
MASK
θ
ΔZ
lm
Artist's conception of various printing techniques. (a) Contact printing, in which wafer is in intimate contact with mask; (b) proximity printing, in which wafer and mask are in close proximity; (c) projection printing, in which light source is scanned across the mask and focused on the wafer.
• Proximity – shadow printing method used to minimize mask damage
• Minimum linewidth or critical dimension $\rightarrow CD = 1m \approx \sqrt{\lambda g}$ g = gap between mask/wafer & includes resist thickness
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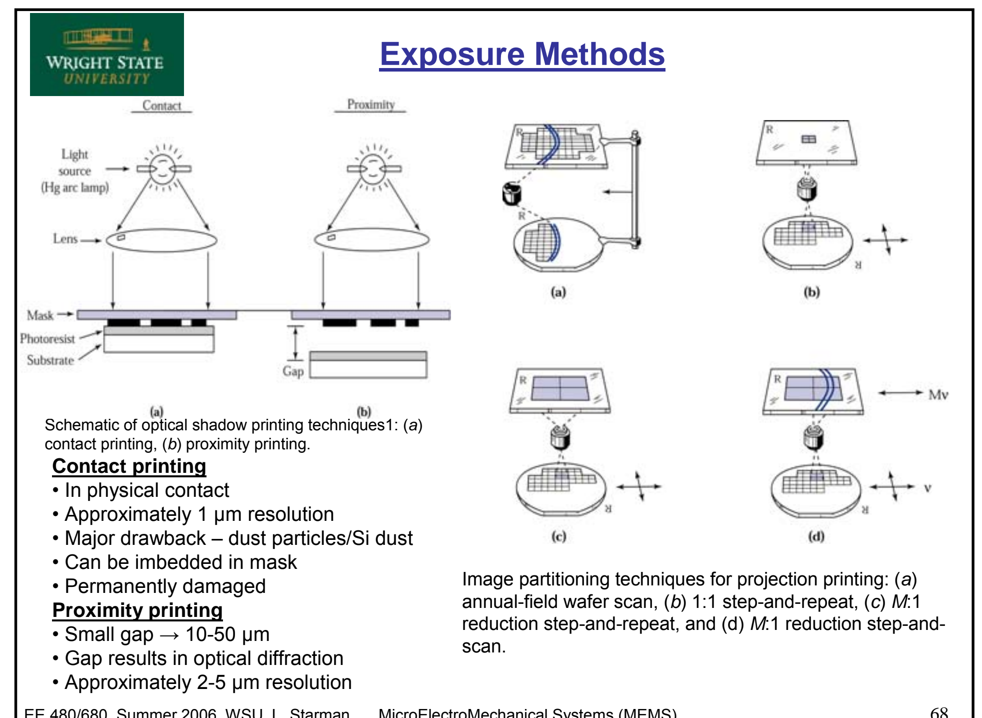
Exposure Methods
WRIGHT STATE UNIVERSITY
Contact
Proximity
Light source (Hg arc lamp)
Lens
Mask
Photoresist
Substrate
Gap
(a)
(b)
Schematic of optical shadow printing techniques1: (a) contact printing, (b) proximity printing.
Contact printing
• In physical contact
• Approximately 1 μm resolution
• Major drawback – dust particles/Si dust
• Can be imbedded in mask
• Permanently damaged
Proximity printing
• Small gap → 10-50 μm
• Gap results in optical diffraction
• Approximately 2-5 μm resolution
(a)
(b)
(c)
(d)
Mv
v
Image partitioning techniques for projection printing: (a) annual-field wafer scan, (b) 1:1 step-and-repeat, (c) M:1 reduction step-and-repeat, and (d) M:1 reduction step-and-scan.
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Projection Printing

Projection Printing

- Avoids the mask damage problem of shadow & contact printing
- Projects image of the mask pattern onto resist-coated wafer
- Many centimeters between mask & wafer
- To increase resolution – only small portion of mask exposed at a time
- Image scanned or stepped across entire wafer
- Resolution of projection system (~ 1 – 0.07 μm) can be calculated by

$$l_m = k_1 \frac{\lambda}{NA} \quad (2)$$

λ= exposure wavelength
k_1 = process dependent factor
NA = numerical aperture

$$NA = \overline{n} \sin\theta \quad (3)$$

where $\overline{n}$ index of refraction in the image medium (usually air, where $\overline{n}$ =1)
θ half-angle of the cone of light converging to a point image at the wafer

Degrees of Freedom (DOF) $$DOF = \frac{\pm l_m / 2}{\tan\theta} \approx \frac{\pm l_m / 2}{\sin\theta} = k_2 \frac{\lambda}{(NA)^2} \quad (4)$$

k_2 = process dependent factor

Lithography Masks

- Used in IC manufacturing
- Use CAD design system to completely describe circuit patterns electrically
- Masks consists of fused silica substrate covered with a chromium layer

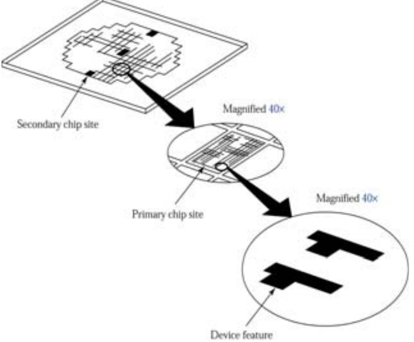


Figure 12.7. An integrated-circuit photomask.[1]

Mask plates – increasing cost & performance
- Low cost glass – emulsion - $100 set
- Quartz , BSG – emulsion, chrome, iron oxide, several thousand $ for set
- Sapphire – $10's of thousand – chrome,

Masks, reticles, and mask making. A tape representing desired pattern is used to generate a reticle containing one cell of the pattern. The reticle pattern is repetitively generated on the substrate, either directly or through intermediate generation of a mask plate.

Exposure Defects/Yield

- Patterns on a mask represent one level of a design
- Typically – 15-20 different masks levels required for a complete IC process cycle
- Standard size mask 15 x 15 cm
- 0.6 cm thick
- Defect density – mask defects
  - Introduced during the manufacture of the mask
  - During subsequent litho processes
- Yield – defined as the ratio of good chips/wafer to the total # of chips/wafer
- Increase yield through
  - inspection
  - Cleaning of masks
  - ultraclean processing area

$$Y \cong e^{-DA}$$

D = average # of fatal defects/unit area
A = area of an IC chip
If D remains the same for all mask levels

$$Y \cong e^{-NDA}$$ N = # of levels

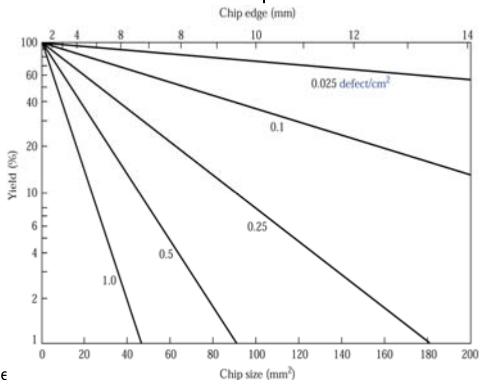


Figure 12.8. Yield for a 10-mask lithographic process with various defect densities per level.

Clean Room

- Integrated circuit fabrication requires a clean processing room
- Dust and other particulates can settle on masks and/in device layers ⇒ causes defects & circuit failure
- Class 100 & below ⇒ workers wear body suits & headgear w/ respirator

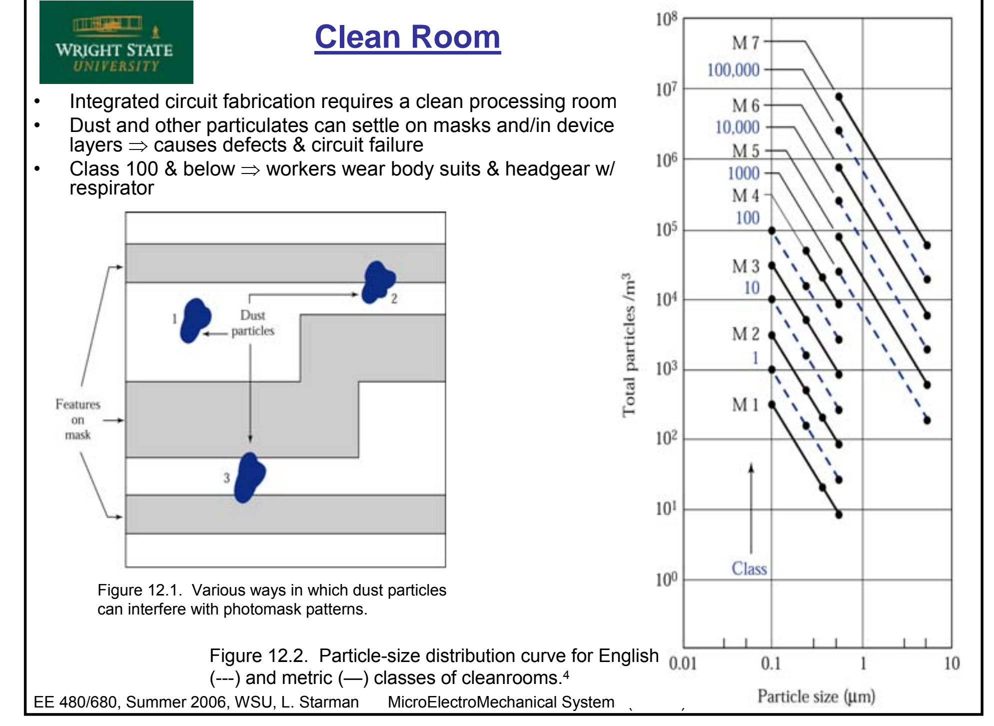
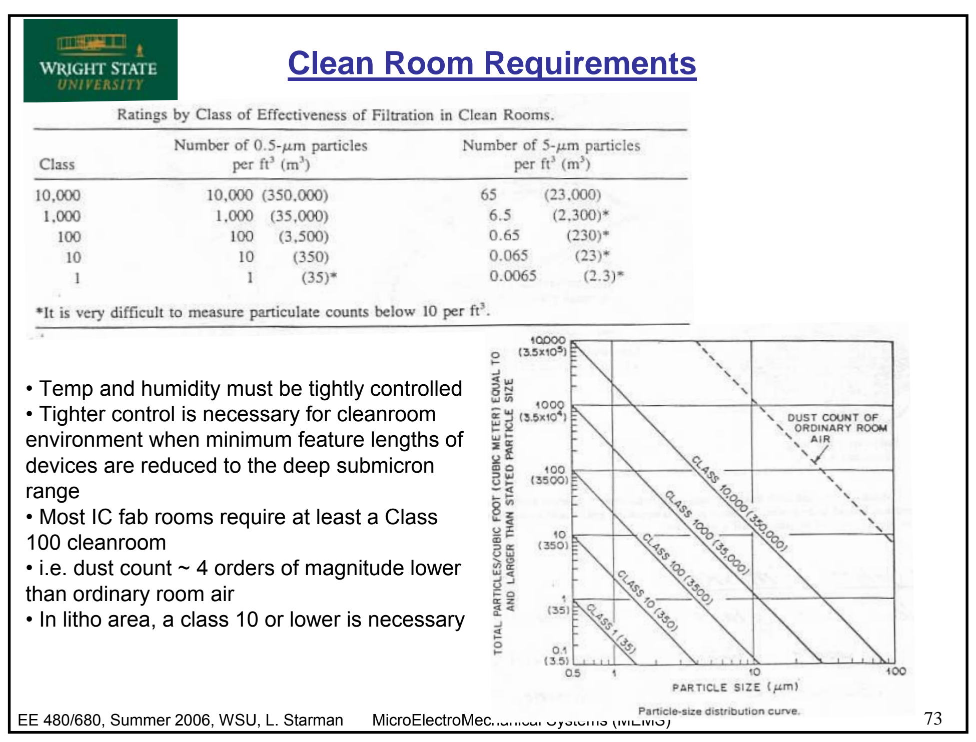


Figure 12.1. Various ways in which dust particles can interfere with photomask patterns.

Figure 12.2. Particle-size distribution curve for English (---) and metric (—) classes of cleanrooms.[4]



Clean Room Requirements

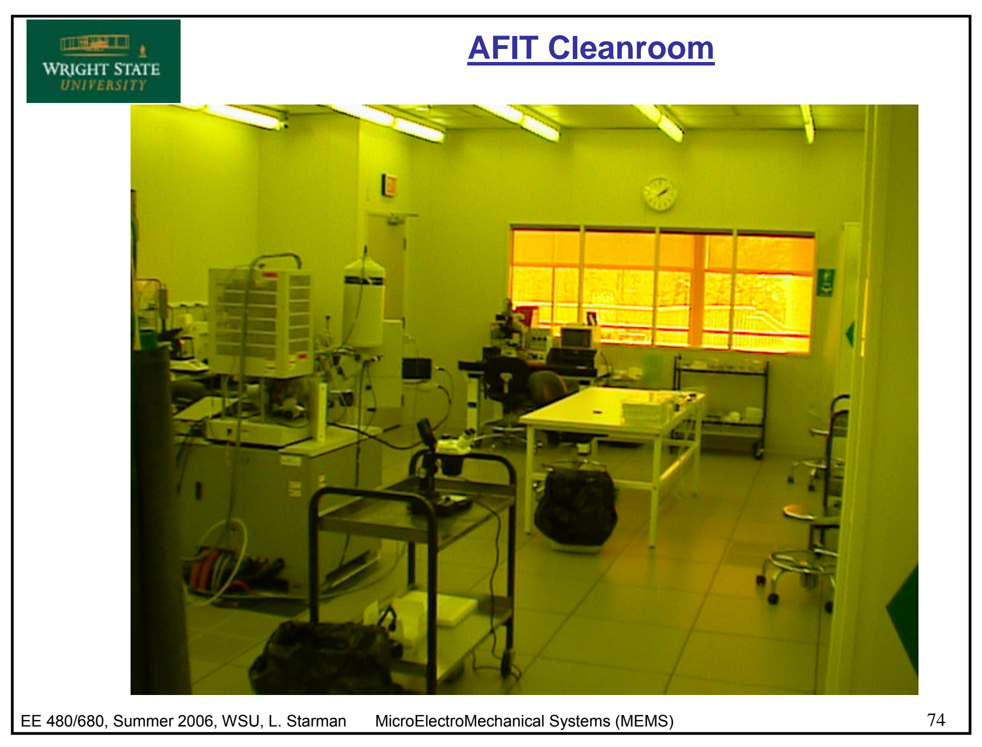
Ratings by Class of Effectiveness of Filtration in Clean Rooms.

Class	Number of 0.5-μm particles per ft³ (m³)	Number of 5-μm particles per ft³ (m³)
10,000	10,000 (350,000)	65 (23,000)
1,000	1,000 (35,000)	6.5 (2,300)*
100	100 (3,500)	0.65 (230)*
10	10 (350)	0.065 (23)*
1	1 (35)*	0.0065 (2.3)*

*It is very difficult to measure particulate counts below 10 per ft³.

- Temp and humidity must be tightly controlled
- Tighter control is necessary for cleanroom environment when minimum feature lengths of devices are reduced to the deep submicron range
- Most IC fab rooms require at least a Class 100 cleanroom
- i.e. dust count ~ 4 orders of magnitude lower than ordinary room air
- In litho area, a class 10 or lower is necessary

Particle-size distribution curve.



AFIT Cleanroom

Photoresist

- Radiation sensitive compound
- Classified as either positive or negative
- **Positive**
  - Exposed regions become more soluble and remove easily in development process
  - Patterns formed (images) are the same as those of the mask
- **Negative**
  - Exposed regions less soluble
  - Patterns formed are the reverse of the mask patterns
- Positive photoresists made up of three components
  - Photosensitive compound – prior to exposure, insoluble in developer solution. After exposure, absorbs radiation & changes chemical structure and become soluble & removable during development
  - Base resin
  - Organic solvent – keeps the resist a fluid/liquid for ease of application
- Negative resists are polymers combined with a photosensitive compound
  - After exposure, absorbs the optical energy and converts it into chemical energy to initiate a polymer linking reaction.
  - Causes crosslinking of polymer molecules which ends up having a higher molecular weight and becomes insoluble in developer solution.
- Major drawback – during development process, whole resist mask swells by absorbing developer solvent. This swelling limits the resolution of negative resist.
- Typical exposure energies for a 1 µm-thick negative resist coating are 10-20 mJ/cm^2
- Negative resist solvents are usually mixtures of hydrocarbons

Photoresist

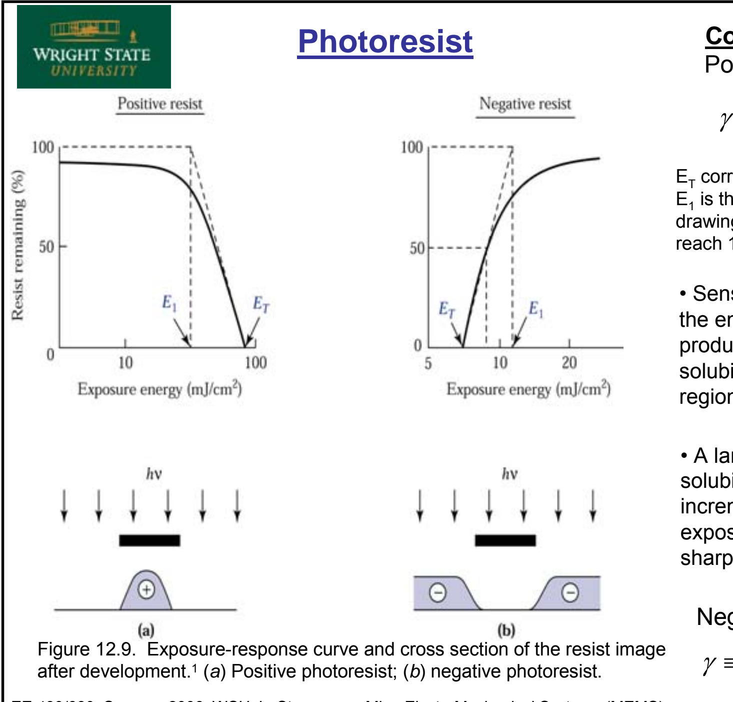


Figure 12.9. Exposure-response curve and cross section of the resist image after development.[1] (*a*) Positive photoresist; (*b*) negative photoresist.

Contrast ratio:

Positive resist:

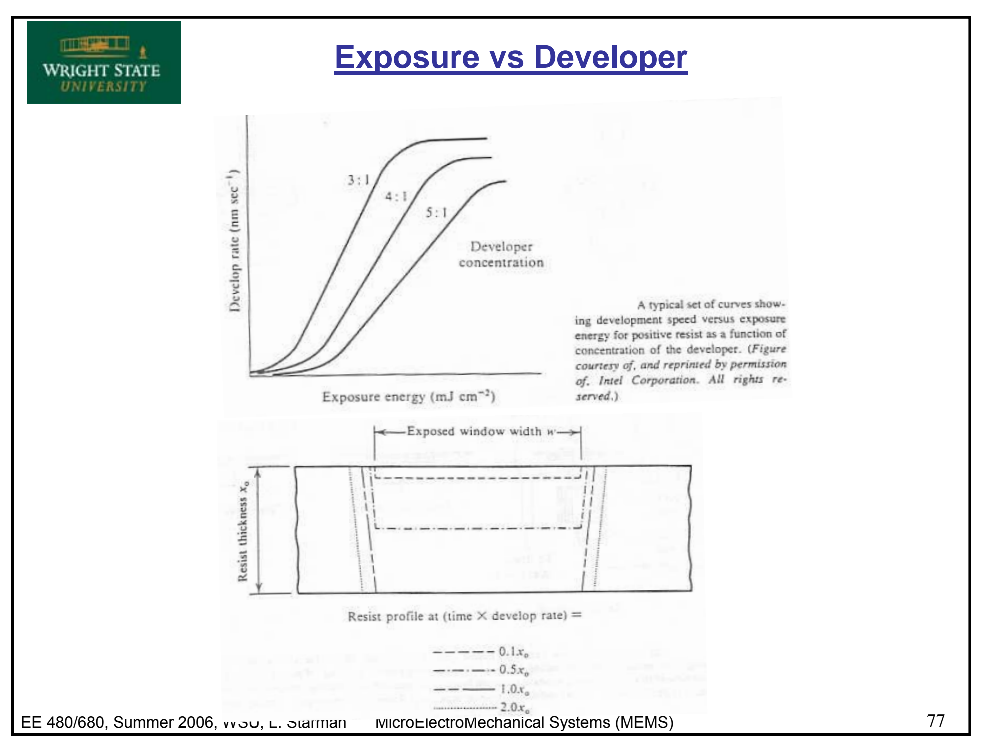
$$\gamma \equiv [\ln(\frac{E_T}{E_1})]^{-1}$$

E_T corresponds to the sensitivity
E_1 is the energy obtained by drawing the tangent at E_T to reach 100% resist thickness

- Sensitivity is defined as the energy required to produce complete solubility in the exposed region
- A larger γ implies a higher solubility of the resist with an incremental increase of exposure energy & results in sharper images

Negative resist:

$$\gamma \equiv [\ln(\frac{E_1}{E_T})]^{-1}$$


Exposure vs Developer
Develop rate (nm sec⁻¹)
3:1
4:1
5:1
Developer concentration
Exposure energy (mJ cm⁻²)
A typical set of curves showing development speed versus exposure energy for positive resist as a function of concentration of the developer. (Figure courtesy of, and reprinted by permission of, Intel Corporation. All rights reserved.)
Exposed window width w
Resist thickness x₀
Resist profile at (time × develop rate) =
0.1x₀
0.5x₀
1.0x₀
2.0x₀
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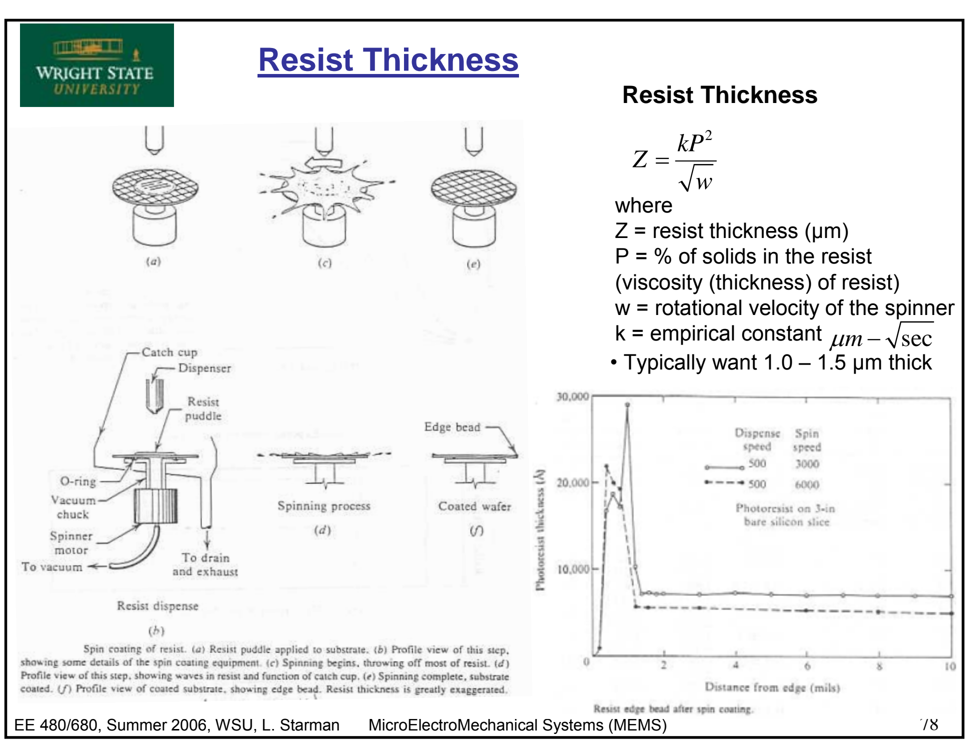
Resist Thickness
Resist Thickness
$Z = \frac{kP^2}{\sqrt{w}}$
where
Z = resist thickness (µm)
P = % of solids in the resist
(viscosity (thickness) of resist)
w = rotational velocity of the spinner
k = empirical constant $\mu m - \sqrt{\sec}$
• Typically want 1.0 – 1.5 µm thick
(a)
(c)
(e)
Catch cup
Dispenser
Resist puddle
O-ring
Vacuum chuck
Spinner motor
To vacuum
To drain and exhaust
Resist dispense
(b)
Spinning process
(d)
Edge bead
Coated wafer
(f)
Spin coating of resist. (a) Resist puddle applied to substrate. (b) Profile view of this step, showing some details of the spin coating equipment. (c) Spinning begins, throwing off most of resist. (d) Profile view of this step, showing waves in resist and function of catch cup. (e) Spinning complete, substrate coated. (f) Profile view of coated substrate, showing edge bead. Resist thickness is greatly exaggerated.
Photoresist thickness (Å)
30,000
20,000
10,000
0
2
4
6
8
10
Distance from edge (mils)
Dispense speed
Spin speed
500
3000
500
6000
Photoresist on 3-in bare silicon slice
Resist edge bead after spin coating.
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Silicon Wafer Cleaning Procedure

Silicon Wafer Cleaning Procedure.

A. Solvent Removal
1. Immerse in boiling trichloroethylene (TCE) for 3 min.
2. Immerse in boiling acetone for 3 min.
3. Immerse in boiling methyl alcohol for 3 min.
4. Wash in DI water for 3 min.

B. Removal of Residual Organic/Ionic Contamination
1. Immerse in a (5:1:1) solution of H_2O–NH_4OH–H_2O_2; heat solution to 75–80 °C and hold for 10 min.
2. Quench the solution under running DI water for 1 min.
3. Wash in DI water for 5 min.

C. Hydrous Oxide Removal
1. Immerse in a (1:50) solution of HF–H_2O for 15 sec.
2. Wash in running DI water with agitation for 30 sec.

D. Heavy Metal Clean
1. Immerse in a (6:1:1) solution of H_2O–HCl–H_2O_2 for 10 min at a temperature of 75–80 °C.
2. Quench the solution under running DI water for 1 min.
3. Wash in running DI water for 20 min.

Generally not performed in this fashion

- **Typical Method**
- Acetone spin 30 sec
- Methanol spin 30 sec
- Isopropyl spin 20 sec
- DI water spin 20 sec
- If Si, dip in BOE for 15 sec
  - Removes native oxides
- DI rinse for 60 + sec
- Dry with N_2

Pattern Transfer

- Cleanroom illuminated with yellow light
  - Why? Photoresists are not sensitive to wavelengths greater than 0.5 µm
- Following cleaning and hotplate bake
- Wafer placed on vacuum spindle
- Liquid photoresist is applied to center of wafer
- Wafer rapidly accelerated up to a constant rotational speed
- Maintained at this speed for ~ 30 sec
- Spin speed generally ranges from 1000-10,000 rpm to coat uniformly
- Resist film thickness about 0.5-1.0 µm
- Resist thickness correlated to its viscosity
- Following spin, wafer placed on hotplate for soft bake (typically 90°-180°C for 60-120 seconds
- Bake used to remove solvents & increase adhesion
- Align wafer with mask and expose to UV
- Develop resist and presto, you have your design pattern – If not, you need remedial training and start over
- Rinse off developer ~60 sec in DI water & dry with N_2
- Continue with deposition/etch processes
- **Inspect fab process continuously under microscope!**
- **NOTE:** each PR will have its own spin speed & developer times and settings

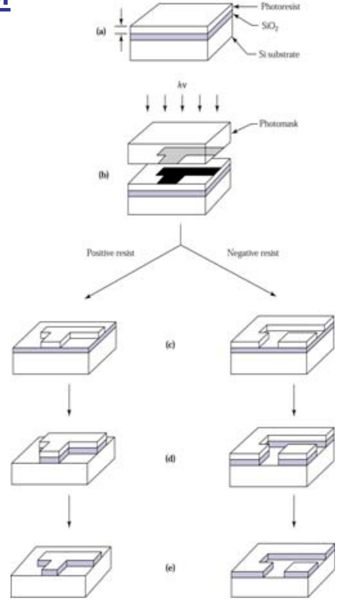
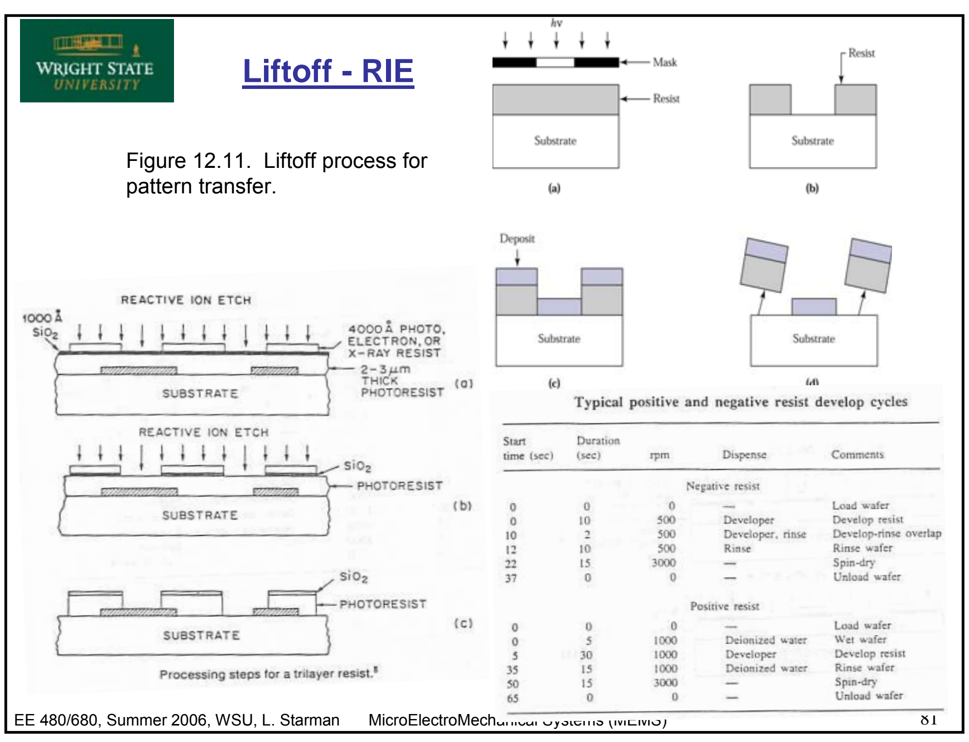
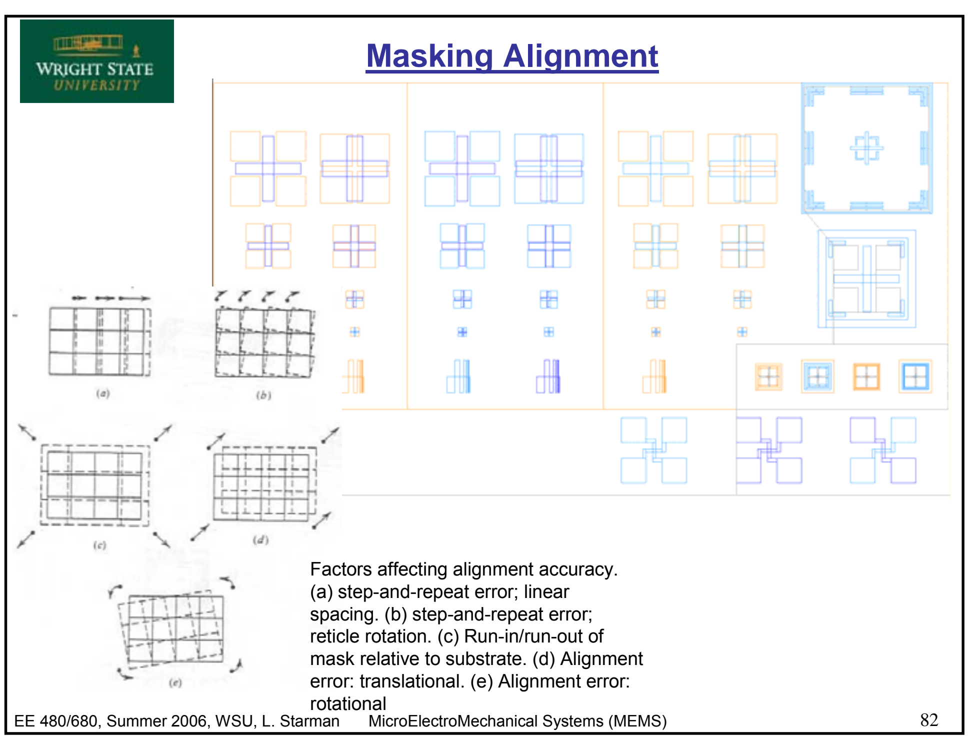


Figure 12.10. Details of the optical lithographic pattern transfer process.



Typical positive and negative resist develop cycles

Start time (sec)	Duration (sec)	rpm	Dispense	Comments
Negative resist				
0	0	0	—	Load wafer
0	10	500	Developer	Develop resist
10	2	500	Developer, rinse	Develop-rinse overlap
12	10	500	Rinse	Rinse wafer
22	15	3000	—	Spin-dry
37	0	0	—	Unload wafer
Positive resist				
0	0	0	—	Load wafer
0	5	1000	Deionized water	Wet wafer
5	30	1000	Developer	Develop resist
35	15	1000	Deionized water	Rinse wafer
50	15	3000	—	Spin-dry
65	0	0	—	Unload wafer



Next Generation Litho Methods

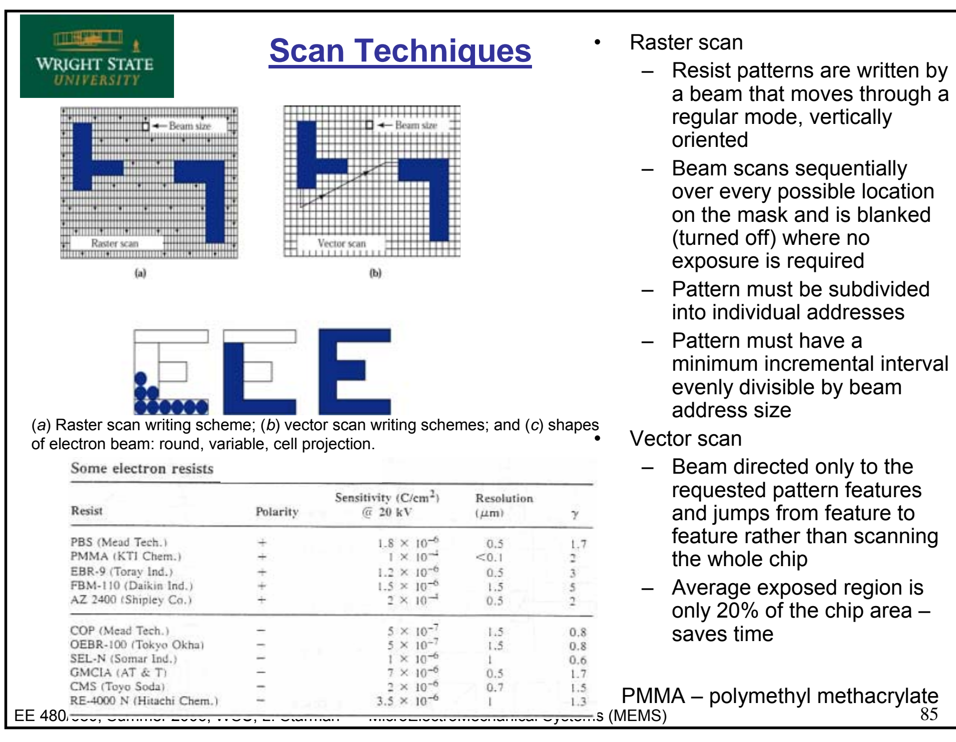
- Optical lithography – widely used due to:
  - High throughput
  - Good resolution
  - Low cost
  - Ease in operation
  - However, limited in deep-submicron IC processes
- Need postoptical lithography to process deep-submicron or even nanometer ICs
- New techniques
  - Electron beam
    - Primarily used to make photomasks
  - X-ray
    - candidate to replace optical lithography, can be used for the fabrication of IC's at 100 nm
  - Ion Beam
    - can achieve the highest resolution, used to repair the masks for optical lithography

Types of advanced lithographic methods. (a) Optical lithography. (b) Electron beam lithography. (c) X-ray lithography. (d) Ion beam lithography.[11]

Electron Beam Lithography

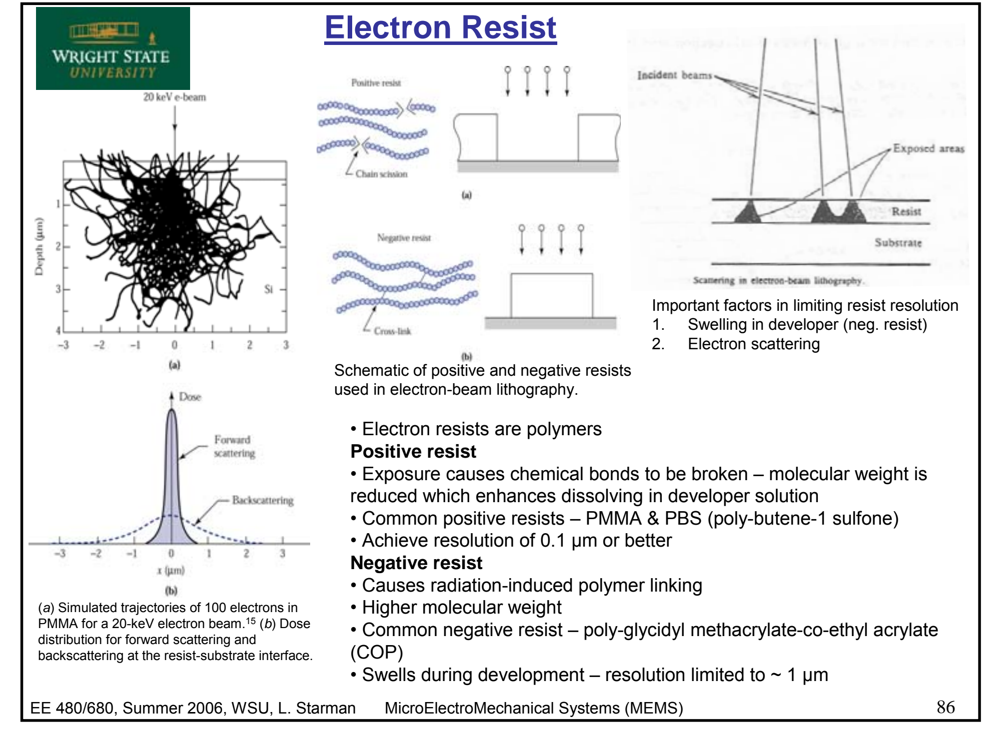
- Electron gun – generates the beam of electrons
- Tungsten thermionic-emission cathode used for electron gun
- Condenser lenses used to focus the electron beam to a spot size 10-25 nm in diameter
- Beam blanking plates turn the electron beam on and off
- Precision mechanical stage used to position the substrate to be patterned
- Advantages
  - Permits generation of submicron resist geometries
  - Highly automated
  - Precisely controlled operation
  - Greater depth of focus
  - Direct patterning on a wafer without using a mask
- Disadvantages
  - Have low throughput ~10 wafers/hr at less that 0.25 µm resolution
  - Fine for mask making

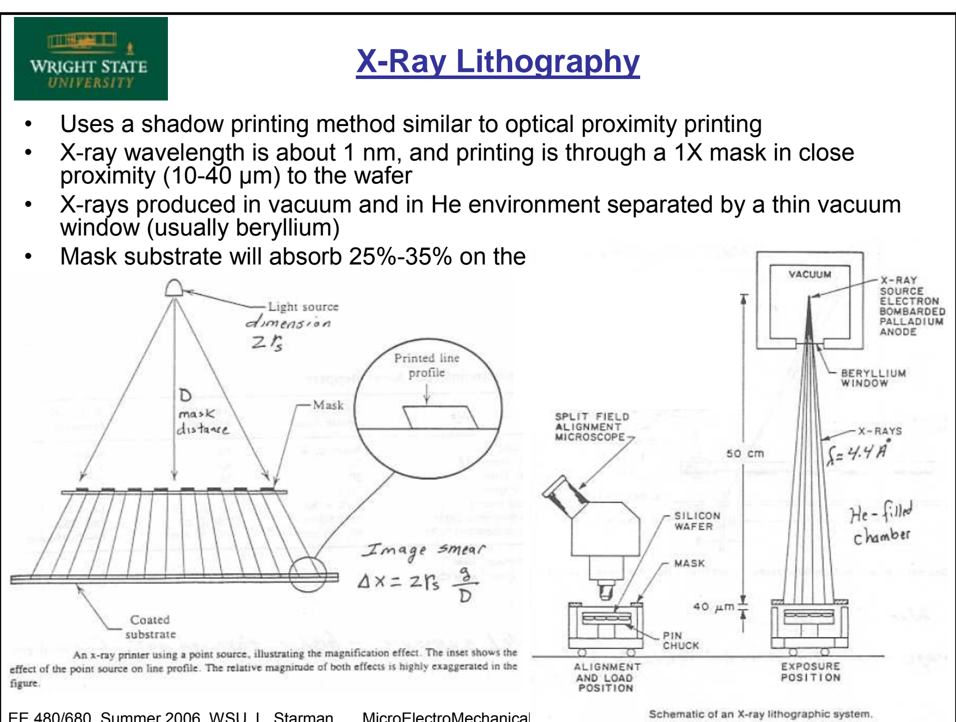
Schematic of an electron-beam machine.



Some electron resists

Resist	Polarity	Sensitivity (C/cm²) @ 20 kV	Resolution (μm)	γ
PBS (Mead Tech.)	+	1.8×10^{-6}	0.5	1.7
PMMA (KTI Chem.)	+	1×10^{-4}	<0.1	2
EBR-9 (Toray Ind.)	+	1.2×10^{-6}	0.5	3
FBM-110 (Daikin Ind.)	+	1.5×10^{-6}	1.5	5
AZ 2400 (Shipley Co.)	+	2×10^{-4}	0.5	2
COP (Mead Tech.)	−	5×10^{-7}	1.5	0.8
OEBR-100 (Tokyo Okha)	−	5×10^{-7}	1.5	0.8
SEL-N (Somar Ind.)	−	1×10^{-6}	1	0.6
GMCIA (AT & T)	−	7×10^{-6}	0.5	1.7
CMS (Toyo Soda)	−	2×10^{-6}	0.7	1.5
RE-4000 N (Hitachi Chem.)	−	3.5×10^{-6}	1	1.3





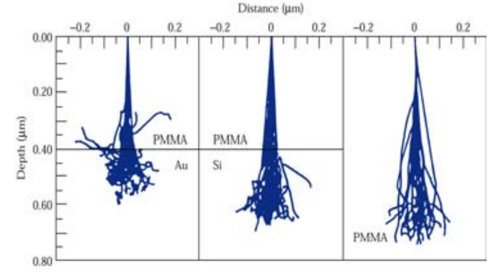
An x-ray printer using a point source, illustrating the magnification effect. The inset shows the effect of the point source on line profile. The relative magnitude of both effects is highly exaggerated in the figure.

Schematic of an X-ray lithographic system.

Ion Beam Lithography

Ion Beam Lithography

- Higher resolution than optical, e-beam, or x-ray lithography
- Higher ion mass ⇒ less scatter
- Use PMMA resist (more sensitive to ions that to e^-s)
- Scanning focused beam or masked beam system
- Ion optics for scanning systems – more difficult to operate than electron optic scanning systems
- Ion source: ionize gas surrounding a W-tip liquid metal flowing to W-tip. Ion current density
  - Ga^+ 0.1 μm spot ⇒ 1.5 A/cm^2
  - H^+ 0.65 μm spot ⇒ 15 A/cm^2
- Must use electrostatic
- (rather than magnetic) "lenses"



Trajectories of 60 keV H^+ ions traveling through PMMA into Au, Si, and PMMA.

Etching

- Two types of etching
  - Wet chemical etching
  - Dry plasma etching
- **Wet etching**
  - Transfer pattern from a resist to a film on a substrate (oxide, epilayer) – or directly to the substrate
  - Proceeds at a relatively slow, controlled rate. Relies on reproducible etch rates with human monitoring
  - Etch rates tend to be limited by the rate of diffusion of the reactant through a stagnant layer that covers the surface
  - Wet etches are often limited by the rate of dissolution of the reaction products into the solution.
  - Agitation of the solution helps to increase the etch rate by enhancing this out diffusion
  - The etching of poly and amorphous materials is isotropic
  - Wet etching of crystalline materials may be isotropic or anisotropic – depending on the nature of the reaction kinetics
  - Isotropic etches ⇒ polishing etches, result in smooth surfaces
  - Used for lapping and polishing to give an optically flat, damage-free surface.

Wet Etching

- Mechanisms for wet chemical etching involve three essential steps
- Reactants are transported by diffusion to the reacting surface
- Chemical reactions occur at the surface
- Products from the surface removed by diffusion
- Both agitation & temperature of the etchant solution will influence the etch rate
- Etching performed by immersion (requires agitation to ensure etch uniformity and consistent etch rate) or spraying the wafers with the etchant solution
- Spray etching replacing immersion etching
  - Increases the etch rate
  - Increases uniformity by constant fresh supply of etchant to wafer
- Etch rate uniformity given by:

$$\text{Etch rate uniformity (\%)} = \frac{\text{(maximum etch rate – minimum etch rate)}}{\text{maximum etch rate + minimum etch rate}} \times 100\%$$

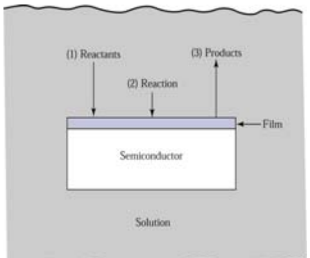


Figure 12.21 Basic mechanisms in wet chemical etching

Oxide Etching

- Buffered oxide etch – commonly used to etch windows in silicon dioxide layers.
- BOE contains HF and a buffer in water
- Room temp (~25°C), BOE etches SiO_2 film much more rapidly than Si or PR
- Depending on the density of the SiO_2 film, etch rate r ~10 to 100 nm/min at RT
- A high concentration of phosphorous in the oxide enhances the etch rate. A reduced etch rate occurs when a high concentration of boron is present (PSG, BSG)
- Length of etch may be controlled visually by monitoring test wafers
- Hydrophobic condition ("beading") indicates completion $\Rightarrow$ HF & H_2O wet silicon dioxide (hydrophilic) but not silicon

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O$$

Buffer HF with ammonium fluoride (NH_4F)

$$NH_4F \rightarrow F^- + NH_4^+$$

Etching profiles obtained with (a) isotropic wet chemical etching and (b) dry anisotropic etching in a plasma or reactive-ion etching system.

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Insulator-Conductor Etchants

Etchants for Insulators and Conductors

Material	Etchant Composition	Etch Rate
SiO_2	28 ml HF, 170 ml H_2O, 113 g NH_4F (Buffered HF)	1000 Å/min
	15 ml HF, 10 ml HNO_3, 300 ml H_2O (P-Etch)	120 Å/min
Si_3N_4	Buffered HF	5 Å/min
	H_3PO_4	100 Å/min
Al	1 ml HNO_3, 4 ml CH_3COOH, 4 ml H_3PO_4, 1 ml H_2O	350 Å/min
Au	4 g KI, 1 g I_2, 40 ml H_2O	1 μm/min
Mo	5 ml H_3PO_4, 2 ml HNO_3, 4 ml CH_3COOH, 150 ml H_2O	0.5 μm/min
Pt	1 ml HNO_3, 7 ml HCl, 8 ml H_2O	500 Å/min
W	34 g KH_2PO_4, 13.4 g KOH, 33 g $K_3Fe(CN)_6$, H_2O to make 1 liter	1600 Å/min

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Etchants for Noncrystalline Films*

Material	Etchant	Remark
SiO_2	28 ml HF 170 ml H_2O 113 g NH_4F	BHF, 1000–2500 Å/min at 25°C
	15 ml HF 10 ml HNO_3 300 ml H_2O	P-etch, 128 Å/min at 25°C
	1 ml BHF 7 ml H_2O	800 Å/min
BSG	1 ml HF 100 ml HNO_3 100 ml H_2O	R-etch, 300 Å/min for 9 mole % B_2O_3, 50 Å/min for SiO_2
	4.4 ml HF 100 ml HNO_3 100 ml H_2O	S-etch, 750 Å/min for 9 mole % B_2O_3, 135 Å/min for SiO_2
PSG	28 ml HF 170 ml H_2O 113 g NH_4F	BHF, 5500 Å/min for 8 mole % P_2O_5
	15 ml HF 10 ml HNO_3 300 ml H_2O	P-etch, 34,000 Å/min for 16 mole % P_2O_5, 110 Å/min for SiO_2
	1 ml BHF 7 ml H_2O	800 Å/min
Si_3N_4	HF	140 Å/min, CVD at 1100°C 750 Å/min, CVD at 900°C 1000 Å/min, CVD at 800°C
	28 ml HF 170 ml H_2O 113 g NH_4F	BHF, 5–10 Å/min
	H_3PO_4	100 Å/min at 180°C
Polysilicon	6 ml HF 100 ml HNO_3 40 ml H_2O	8000 Å/min, smooth edges
	1 ml HF 26 ml HNO_3 33 ml CH_3COOH	1500 Å/min
SIPOS	1 ml HF 6 ml H_2O 10 ml NH_4F (40%)	2000 Å/min for 20% O_2 film

Etch Rates

- Rate determining step (slowest reaction step)
- Rule of thumb – reaction rates double with every 10°C of increased temperature
- Thus ±1°C can change etch rates ~10%, and temperature control is important in etching reactions
- Etching of crystalline silicon
- Wet etching proceeds by oxidation, followed by the dissolution of the oxide by a chemical reaction
- Common etchants for silicon

HNO_3 (nitric acid) + HF (hydrofluoric acid) in H_2O or CH_3COOH (acetic acid)

$Si + 2H^+ \rightarrow Si^{2+}$ (auto catalytic process) higher oxidation state
Oxidizing specie (OH^-) formed by the dissociation of H_2O

$$H_2O \rightleftharpoons OH^- + H^+$$

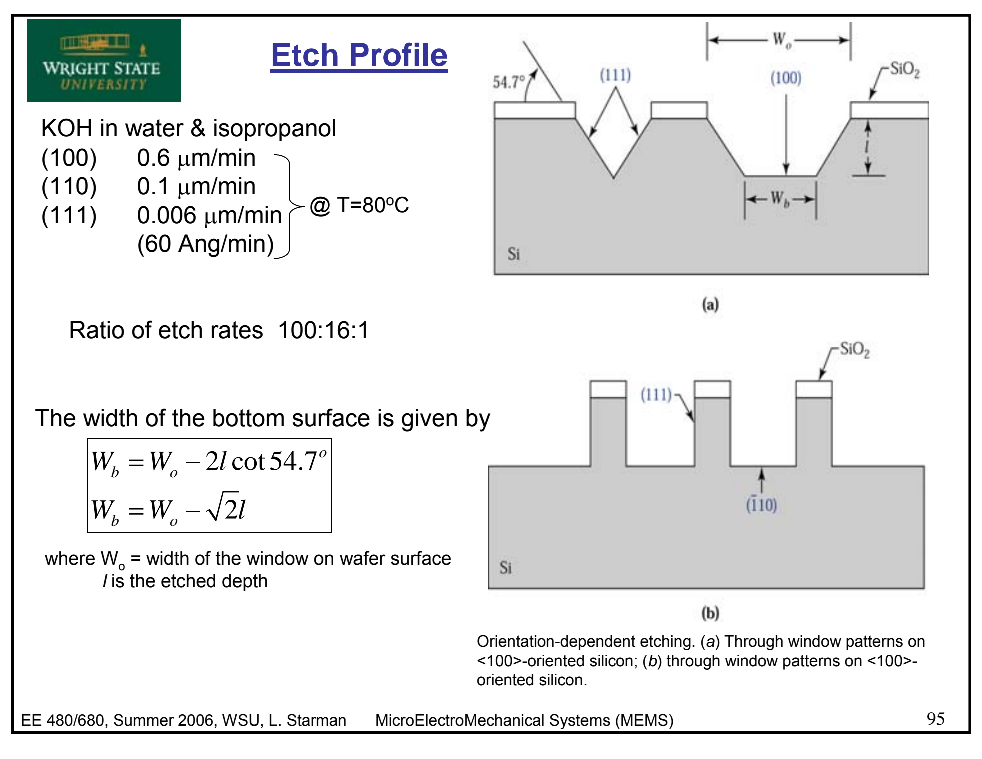
$$Si^{2+} + 2OH^- \rightarrow Si(OH)_2 \rightarrow SiO_2 + H_2$$ liberates H_2

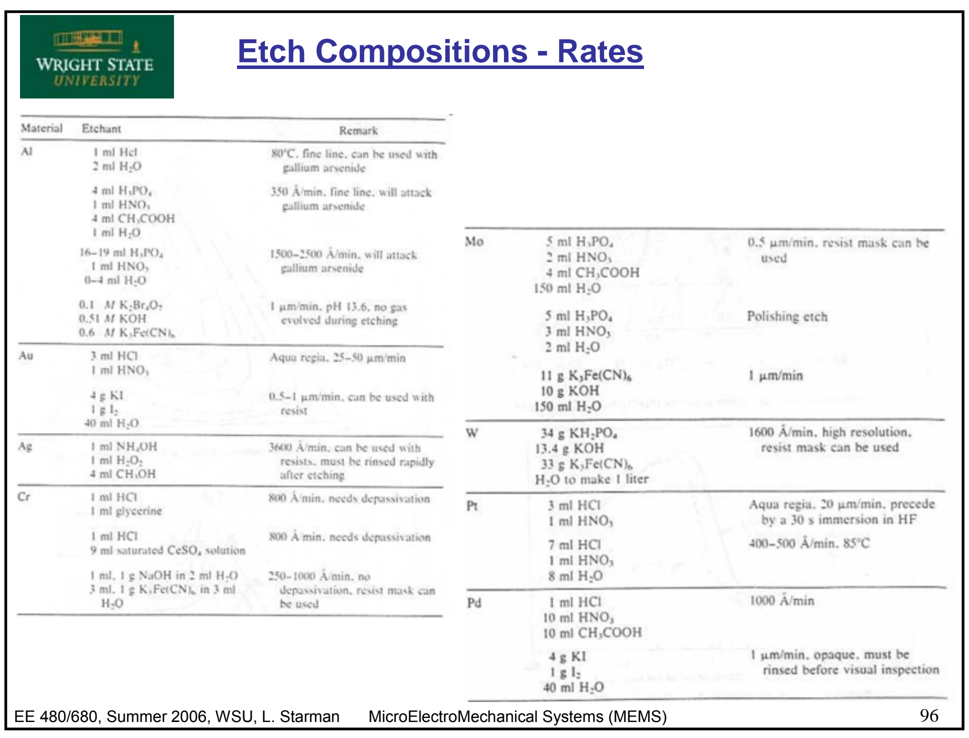
The HF is used to dissolve SiO_2

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

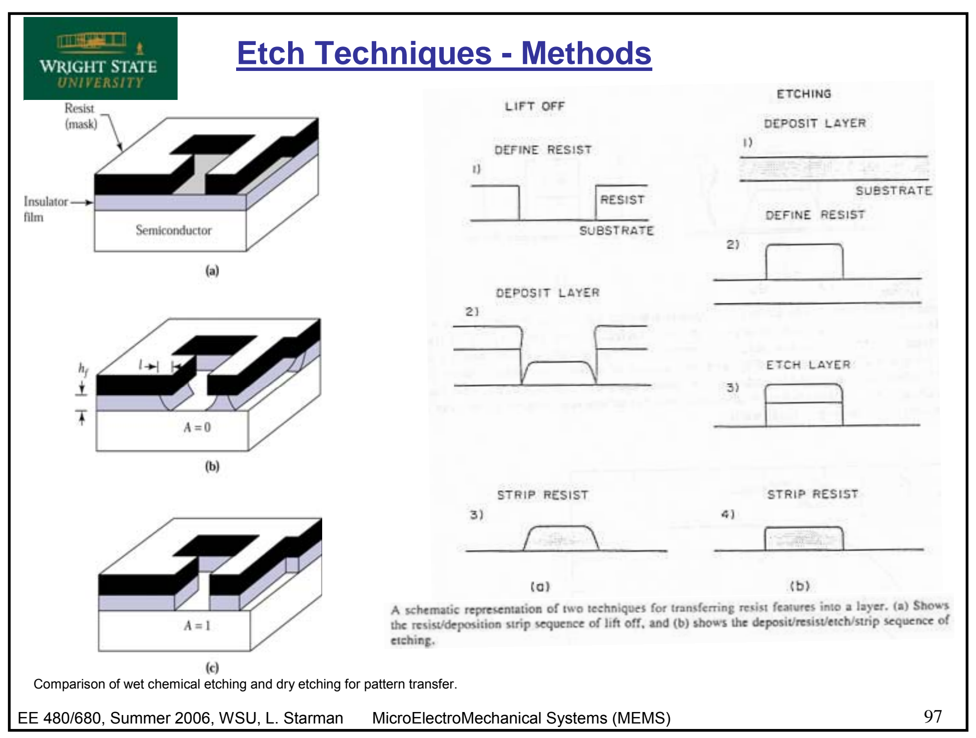
Takes place in MEMS process to remove SiO_2

Soluble in water





Material	Etchant	Remark
Al	1 ml Hcl 2 ml H_2O	80°C, fine line, can be used with gallium arsenide
	4 ml H_3PO_4 1 ml HNO_3 4 ml CH_3COOH 1 ml H_2O	350 Å/min, fine line, will attack gallium arsenide
	16–19 ml H_3PO_4 1 ml HNO_3 0–4 ml H_2O	1500–2500 Å/min, will attack gallium arsenide
	0.1 *M* $K_2Br_4O_7$ 0.51 *M* KOH 0.6 *M* $K_3Fe(CN)_6$	1 μm/min, pH 13.6, no gas evolved during etching
Au	3 ml HCl 1 ml HNO_3	Aqua regia, 25–50 μm/min
	4 g KI 1 g I_2 40 ml H_2O	0.5–1 μm/min, can be used with resist
Ag	1 ml NH_4OH 1 ml H_2O_2 4 ml CH_3OH	3600 Å/min, can be used with resists, must be rinsed rapidly after etching
Cr	1 ml HCl 1 ml glycerine	800 Å/min, needs depassivation
	1 ml HCl 9 ml saturated $CeSO_4$ solution	800 Å/min, needs depassivation
	1 ml, 1 g NaOH in 2 ml H_2O 3 ml, 1 g $K_3Fe(CN)_6$ in 3 ml H_2O	250–1000 Å/min, no depassivation, resist mask can be used
Mo	5 ml H_3PO_4 2 ml HNO_3 4 ml CH_3COOH 150 ml H_2O	0.5 μm/min, resist mask can be used
	5 ml H_3PO_4 3 ml HNO_3 2 ml H_2O	Polishing etch
	11 g $K_3Fe(CN)_6$ 10 g KOH 150 ml H_2O	1 μm/min
W	34 g KH_2PO_4 13.4 g KOH 33 g $K_3Fe(CN)_6$ H_2O to make 1 liter	1600 Å/min, high resolution, resist mask can be used
Pt	3 ml HCl 1 ml HNO_3	Aqua regia, 20 μm/min, precede by a 30 s immersion in HF
	7 ml HCl 1 ml HNO_3 8 ml H_2O	400–500 Å/min, 85°C
Pd	1 ml HCl 10 ml HNO_3 10 ml CH_3COOH	1000 Å/min
	4 g KI 1 g I_2 40 ml H_2O	1 μm/min, opaque, must be rinsed before visual inspection



Dry Etching Summation

- Major disadvantage of wet chemical etching for pattern transfer is the undercutting of the layer under the mask, results in loss of resolution in etched pattern.
- In practice, for isotropic etching, the film thickness should be about one-third or less of the resolution required
- If patterns are required for resolutions much smaller than the film thickness, anisotropic etching must be used
- Dry etching techniques include:
  - Plasma etching
    - fully or partially ionized gas composed of equal #'s of positive & negative charges & a different # of unionized molecules
    - Produced when an E-field of sufficient magnitude is applied to a gas, causing the gas to break down & become ionized
  - Reactive ion etching (RIE)
    - Extensively used in microelectronic industry
    - Uses parallel-plate diode system, RF capacitive-coupled bottom electrode which holds the wafer.
    - Low etch selectivity when compared to traditional barrel etch systems
  - Sputter etching
  - High density plasma (HDP) etching

Impurity Overview

- Basic diffusion process
  - under high temp & high concentration-gradient conditions
- Extrinsic diffusion
  - impurity profiles for constant diffusivity & concentration-dependent diffusivity
- Diffusion related processes
  - impact of lateral diffusion
- Range of implanted ions
  - process & advantages
- Implant damage & annealing
  - ion distribution in crystal lattice & how to remove lattice damage
- Implant related processes
  - masking, high-energy implantation, and high current implantation

Diffusion Doping

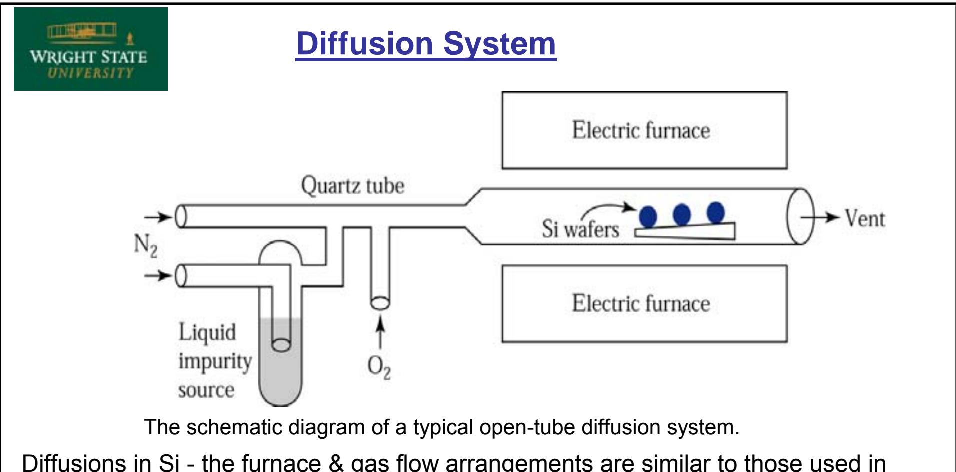
- Diffusion (and ion implantation) provides an important means of introducing controlled amounts of chemical impurities (dopants) into the lattice of a crystalline semiconductor substrate
- Diffusion is used for pn junctions, bipolar transistors, n-tubs for CMOS, selectively disordering regions of lasers, ohmic contact formation, et al.
- In practice, semiconductor wafers are placed in a furnace and an inert gas (N_2) that contains the desired dopant is passed over the wafers. In addition to gaseous dopant sources, liquid and solid sources are used
- Diffusion
  - slowly & high temp
- Ion implant
  - Gaussian distribution func.
  - Fast & at room temp
  - Peak – dependent on incident ion energy
  - Anneal ions to activate them

Gas of dopant atoms — Mask — lnC — x — (a)

High-velocity dopant ions — Mask — lnC — x — (b)

Comparison of (*a*) diffusion and (*b*) ion-implantation techniques for the selective introduction of dopants into the semiconductor substrate.

Diffusion System



The schematic diagram of a typical open-tube diffusion system.

Diffusions in Si - the furnace & gas flow arrangements are similar to those used in oxidation systems.

Diffusions in GaAs are done in sealed ampules containing an As overpressure or open-tube furnace with a doped oxide capping layer (SiN). Overpressure to prevent the loss of As by decomposition or evaporation.

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

Chemical reaction for phosphorus diffusion using liquid source

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$$

P_2O_5 forms a glass on Silicon wafer & then reduced to P by Silicon

Silicon Diffusion Implementation

- 800-1200°C
- P-type (B)
  - BN - boron nitride (solid)
  - BBr_3 - boron bromide (liquid)
  - B_2H_6 - diborane (gas)
- N-type (As/P)
  - As_2O_3 - arsenic trioxide (solid)
  - P_2O5 - phosphorous pentoxide (solid)
  - $AsCl_3$ - arsenic trichloride
  - $POCl_3$ - phosphorous oxychloride
  - AsH_3 - arsine
  - PH_3 – phosphine
- All dopants have solid solubilities
  - > 5E20 cm^{-3} at the temperatures of interest

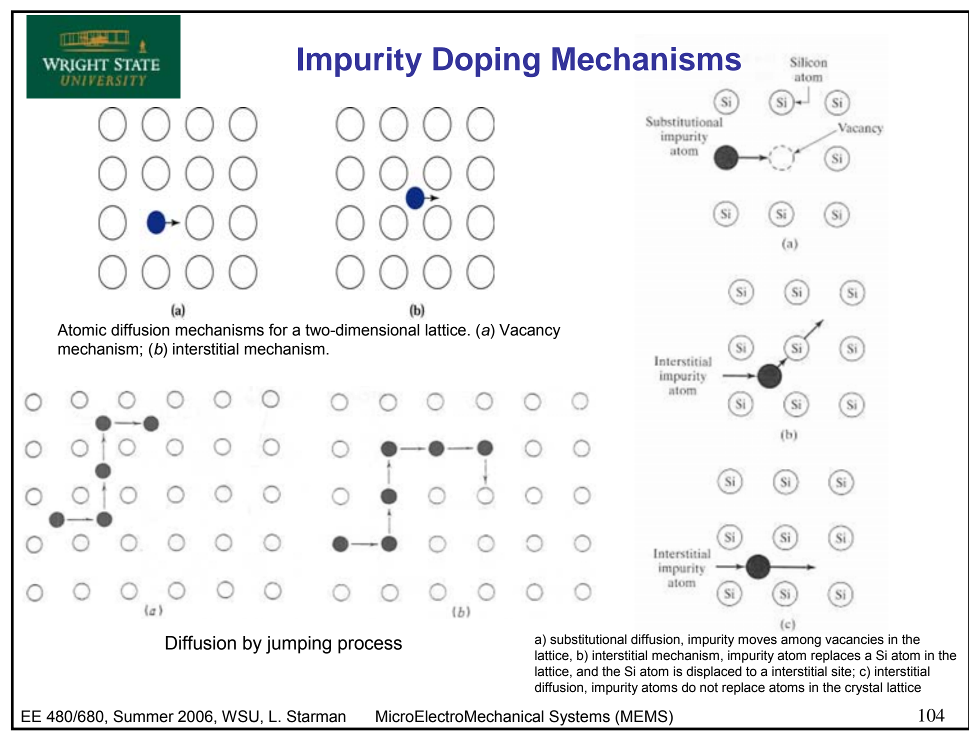
Mechanisms of Diffusion and Doping

- Diffusion describes the process by which atoms move in a crystal lattice
- Although this includes self-diffusion, our primary interest is the diffusion of impurity atoms that are introduced into the lattice for the purpose of altering its electronic properties
- Concentration gradients, temperature, geometrical features (orientation, defect densities), and bonding strengths play an important role in the diffusion process
- The wandering of impurities in a lattice takes place by a series of “random” jumps in three dimensions
- A flux of diffusing species results if there is a concentration gradient
- Interstitial Diffusion
- Substitutional Diffusion
- Interchange Diffusion

} primary mechanisms for diffusion

- Combination Effects
- Diffusion is fast if some defects are present in the crystal

Impurity Doping Mechanisms



Atomic diffusion mechanisms for a two-dimensional lattice. (*a*) Vacancy mechanism; (*b*) interstitial mechanism.

Diffusion by jumping process

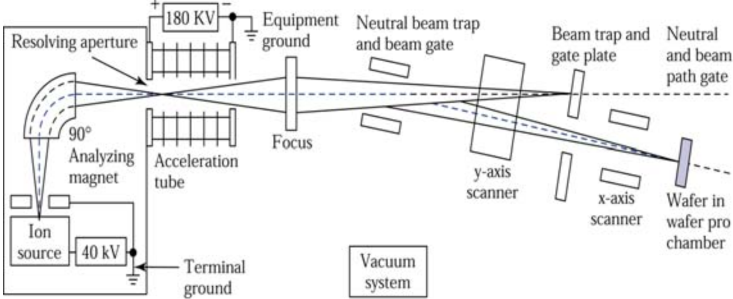
a) substitutional diffusion, impurity moves among vacancies in the lattice, b) interstitial mechanism, impurity atom replaces a Si atom in the lattice, and the Si atom is displaced to a interstitial site; c) interstitial diffusion, impurity atoms do not replace atoms in the crystal lattice

Impurity Doping Mechanisms

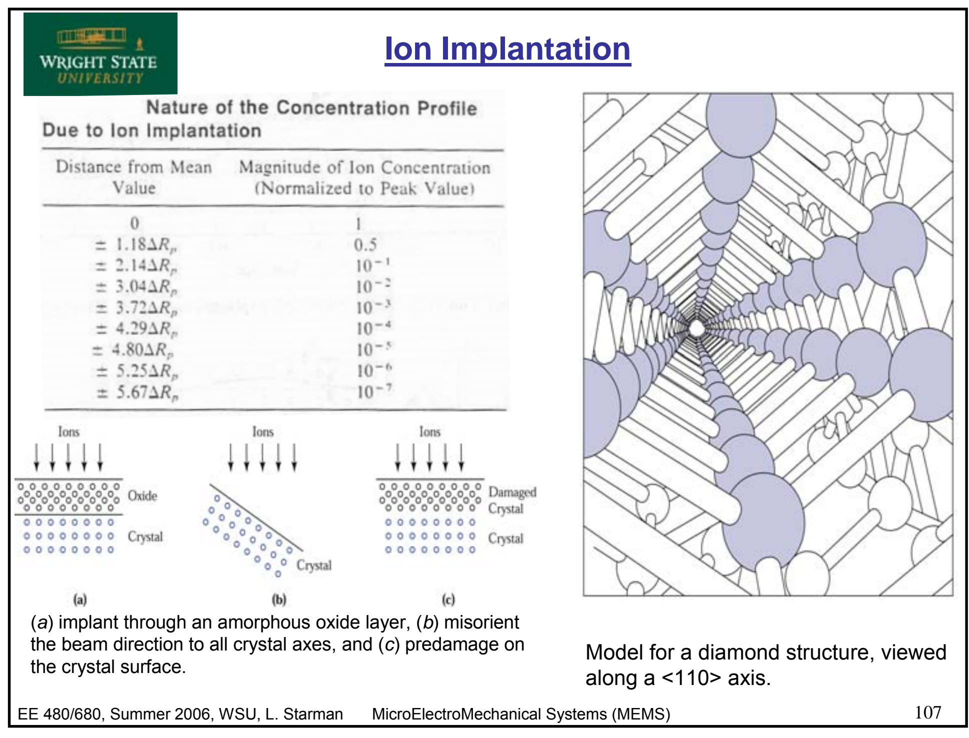
- Vacancy or substitutional
  - Impurity atoms wander through he crystal by jumping from one lattice site to the next, substituting for the original host atom. It is necessary that this adjacent site be vacant
  - **vacancies must be present to allow substitutional diffusion to occur**
  - Will not occur in a perfect crystal
- Interstitial Diffusion
  - impurity atoms move through the crystal by jumping from one interstitial site to the next. They may start at either lattice or interstitial sites and may end up in either type of site.
  - **interstitial diffusion requires that their jump motion occur from one interstitial site to another adjacent interstitial site.**
  - Can occur in a perfect crystal
- Dissociative Mechanism
  - substitutional atom can become an interstitial (occupy both sites)
  - This mechanism may control diffusion
    - Cu, Ni, Au in Si
    - Zn, Cd, Cu in GaAs
- Interchange diffusion
  - two or more atoms diffuse by an interchange process.
  - direct interchange involves two atoms and a cooperative interchange involves a large number of atoms .
  - The probability of interchange diffusion is relatively low.
- Combination Effects
  - as name implies, a fraction of the impurity atoms may diffuse substitutionally and the rest interstitially (two stream process).
  - some diffusion atoms may end up in substitutional sites, others in interstitial sites.

Ion Implantation

- A useful alternative to high temperature diffusion for doping (target wafer held at low temp)
- Impurity gas (BF_3, AsH_3, O_2, etc.) is ionized via a high voltage accelerator
- Beam of ionized impurity atoms (plus molecular fragments) with ~ 1 cm diameter is generated
- Beam current is ~10 µA to 1 mA, giving a charge Q transported down a "linear accelerator"
- Implant dose range 10^{12} to 10^{18} atoms/cm^2
- Good for making small devices
- Typical ion energies 30 to 300 KeV – up to ~ 1 MeV
- Average depths ranging from 10 nm to 10 µm
- Advantages: precise control and reproducibility of impurity dopings and its lower processing temperature

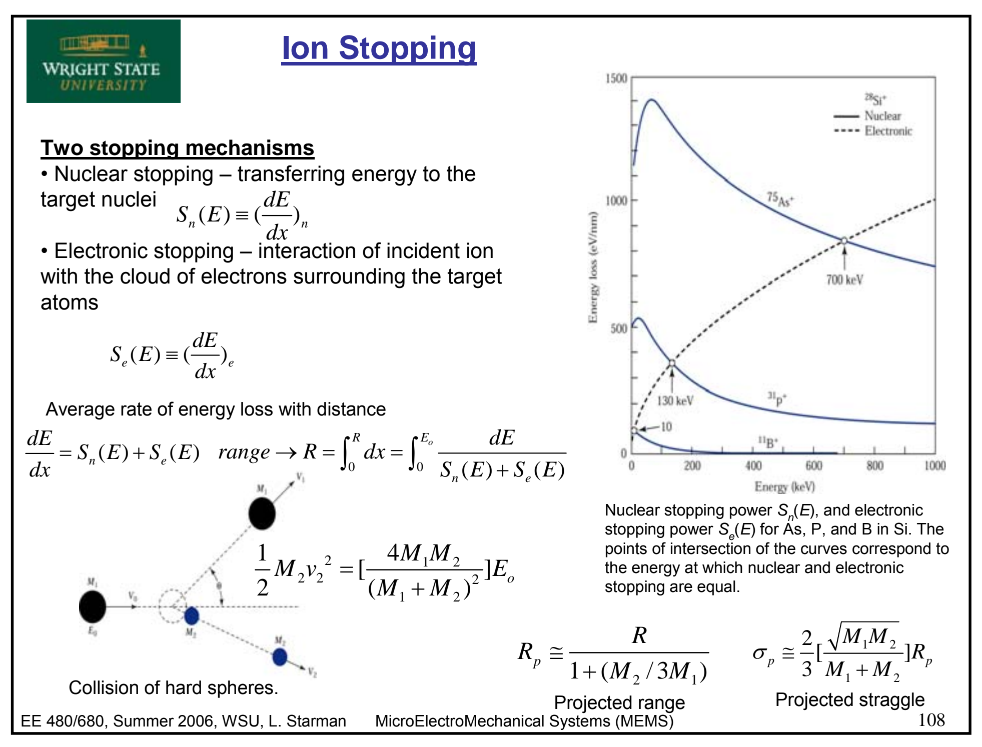


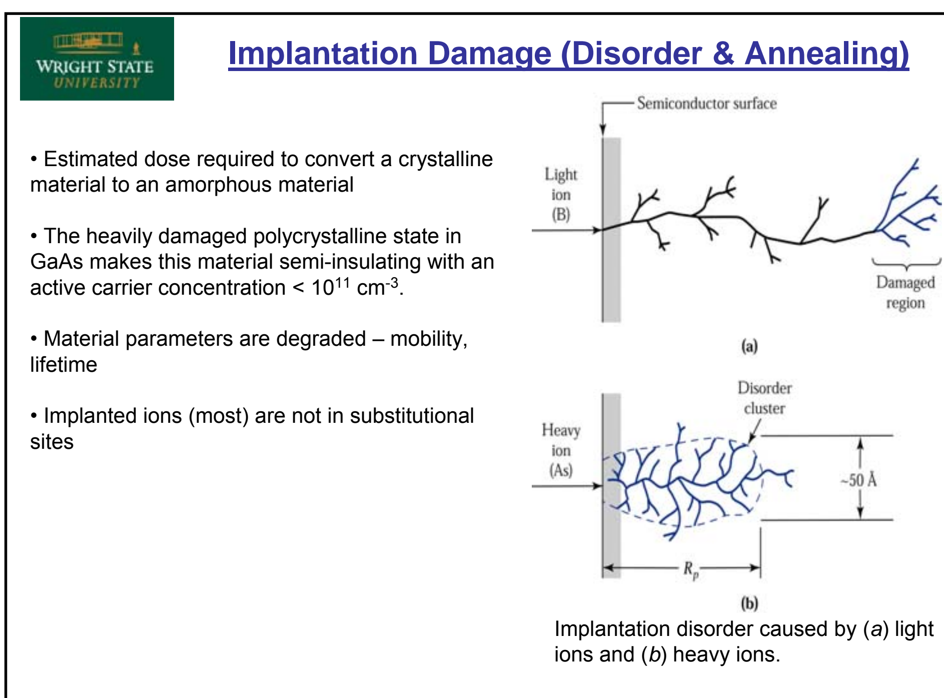
Schematic of a medium-current ion implantor.



Nature of the Concentration Profile Due to Ion Implantation

Distance from Mean Value	Magnitude of Ion Concentration (Normalized to Peak Value)
0	1
$\pm\ 1.18\Delta R_p$	0.5
$\pm\ 2.14\Delta R_p$	10^{-1}
$\pm\ 3.04\Delta R_p$	10^{-2}
$\pm\ 3.72\Delta R_p$	10^{-3}
$\pm\ 4.29\Delta R_p$	10^{-4}
$\pm\ 4.80\Delta R_p$	10^{-5}
$\pm\ 5.25\Delta R_p$	10^{-6}
$\pm\ 5.67\Delta R_p$	10^{-7}

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Implantation Damage (Disorder & Annealing)
• Estimated dose required to convert a crystalline material to an amorphous material
• The heavily damaged polycrystalline state in GaAs makes this material semi-insulating with an active carrier concentration < 10^11 cm^-3.
• Material parameters are degraded – mobility, lifetime
• Implanted ions (most) are not in substitutional sites
Semiconductor surface
Light ion (B)
Damaged region
(a)
Disorder cluster
Heavy ion (As)
~50 Å
Rp
(b)
Implantation disorder caused by (a) light ions and (b) heavy ions.
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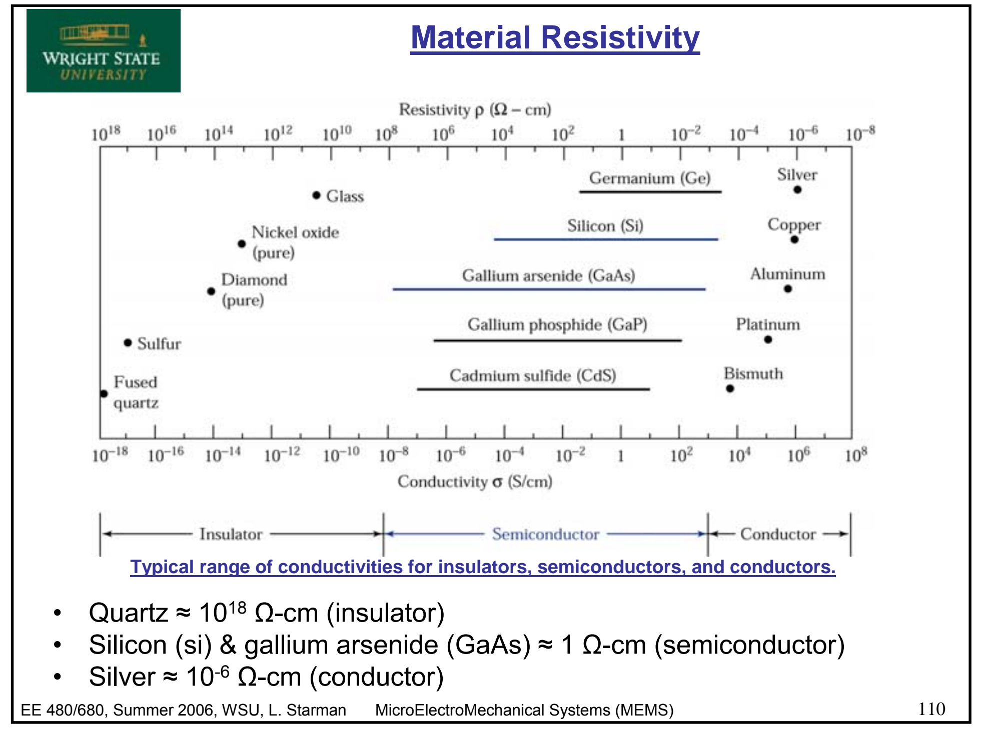
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Material Resistivity
Resistivity ρ (Ω – cm)
10^18 10^16 10^14 10^12 10^10 10^8 10^6 10^4 10^2 1 10^-2 10^-4 10^-6 10^-8
Glass
Nickel oxide (pure)
Diamond (pure)
Sulfur
Fused quartz
Germanium (Ge)
Silicon (Si)
Gallium arsenide (GaAs)
Gallium phosphide (GaP)
Cadmium sulfide (CdS)
Silver
Copper
Aluminum
Platinum
Bismuth
10^-18 10^-16 10^-14 10^-12 10^-10 10^-8 10^-6 10^-4 10^-2 1 10^2 10^4 10^6 10^8
Conductivity σ (S/cm)
Insulator
Semiconductor
Conductor
Typical range of conductivities for insulators, semiconductors, and conductors.
• Quartz ≈ 10^18 Ω-cm (insulator)
• Silicon (si) & gallium arsenide (GaAs) ≈ 1 Ω-cm (semiconductor)
• Silver ≈ 10^-6 Ω-cm (conductor)
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Resistivity, Conductivity

Figure 3.5. Current conduction in a uniformly doped semiconductor bar with length *L* and cross-sectional area *A*.

Electric field is: $E = \frac{1}{q}\frac{dE_C}{dx}$ (V/cm)

Electron current $I_n = qnA\upsilon_n \quad \upsilon_n = -\mu_n E$

TABLE 1 Portion of the Periodic Table Related to Semiconductors

Period	Column II	III	IV	V	VI
2		B Boron	C Carbon	N Nitrogen	O Oxygen
3	Mg Magnesium	Al Aluminum	Si Silicon	P Phosphorus	S Sulfur
4	Zn Zinc	Ga Gallium	Ge Germanium	As Arsenic	Se Selenium
5	Cd Cadmium	In Indium	Sn Tin	Sb Antimony	Te Tellurium
6	Hg Mercury		Pb Lead		

Ohm's Law: $J = \sigma E = \frac{1}{\rho}E$

J = the current density (A/cm^2)

• Current density is proportional to the E-field

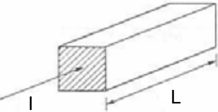
$\rho \equiv resistivity \quad \Omega \cdot cm$

$\sigma \equiv conductivity \, (\Omega \cdot cm)^{-1}$

Derivation

Sheet-Resistance Definition

Resistance R of the rectangular block of uniformly doped material shown below



$$R = \frac{\rho L}{A} \qquad Area = tW$$

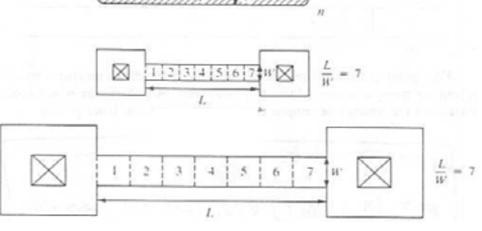
where ρ = material's resistivity
L = length of block
A = cross-sectional area of block

$$R = (\frac{\rho}{t})(\frac{L}{W}) = R_s(\frac{L}{W})$$

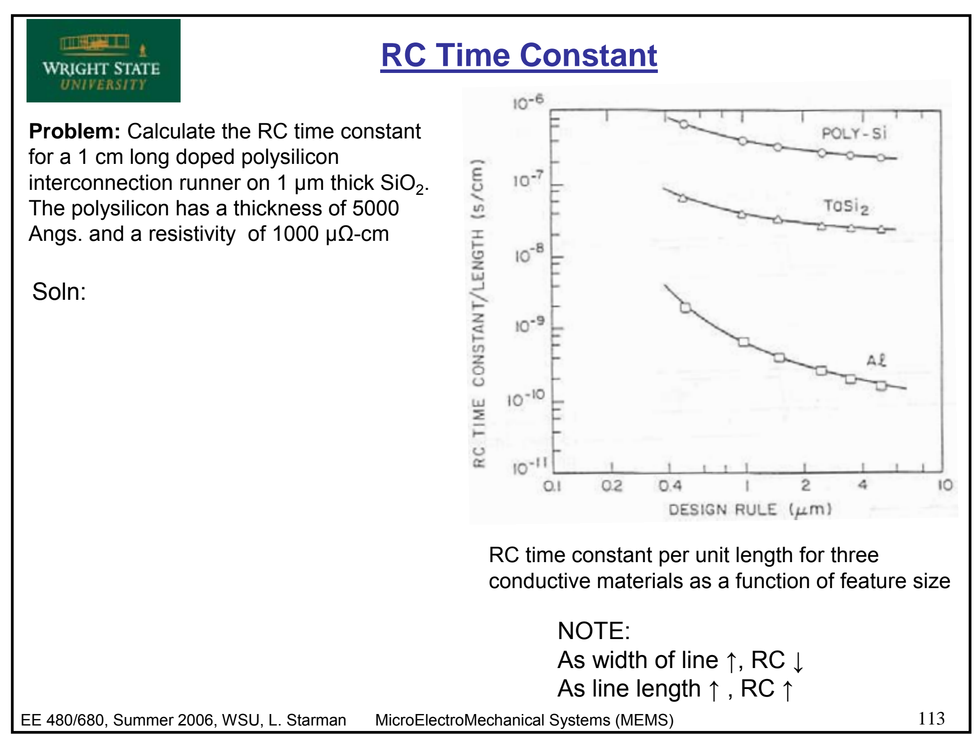
where R_s = (ρ/t) is called the **sheet resistance** of the layer of material

$\rho = (\frac{1}{\sigma})$ and $\sigma = q(\mu_n n + \mu_p p)$

Sheet resistance of a material is the ratio of resistivity to thickness



Top and side views of two diffused resistors of different physical size having equal values of R. Each resistor has a ratio L/W equal to 7 squares. Each end of the resistor contributes approximately 0.65 additional squares


RC Time Constant
Problem: Calculate the RC time constant for a 1 cm long doped polysilicon interconnection runner on 1 μm thick SiO_2. The polysilicon has a thickness of 5000 Angs. and a resistivity of 1000 μΩ-cm
Soln:
RC TIME CONSTANT/LENGTH (s/cm)
DESIGN RULE (μm)
POLY-Si
TaSi2
Al
RC time constant per unit length for three conductive materials as a function of feature size
NOTE:
As width of line ↑, RC ↓
As line length ↑ , RC ↑
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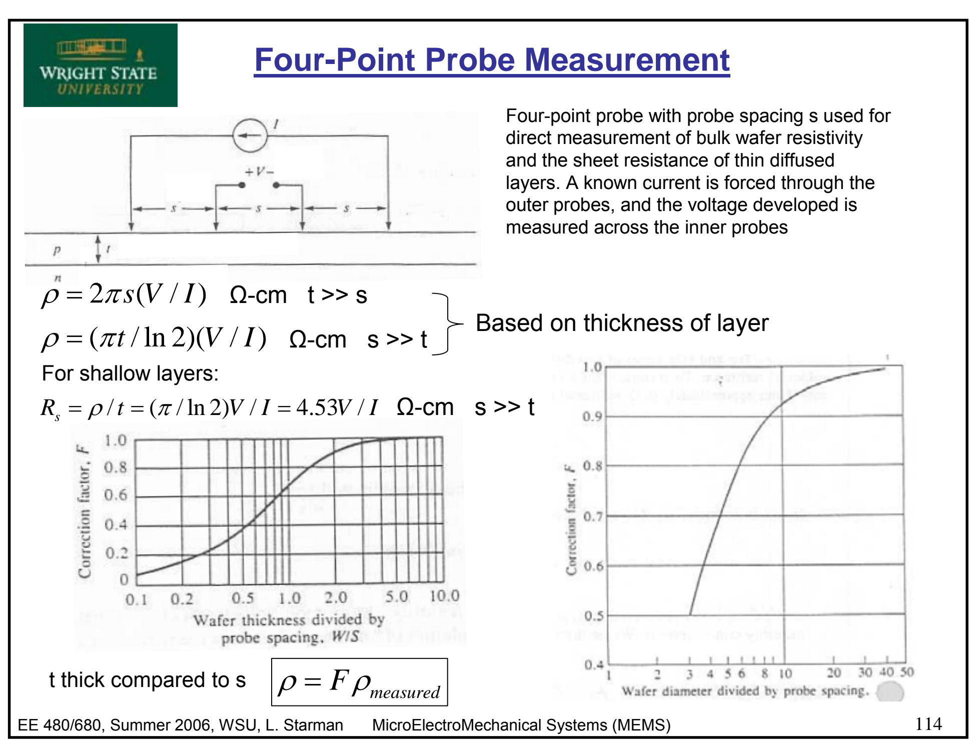
Four-Point Probe Measurement
Four-point probe with probe spacing s used for direct measurement of bulk wafer resistivity and the sheet resistance of thin diffused layers. A known current is forced through the outer probes, and the voltage developed is measured across the inner probes
$\rho = 2\pi s(V/I)$ Ω-cm t >> s
$\rho = (\pi t/\ln 2)(V/I)$ Ω-cm s >> t
Based on thickness of layer
For shallow layers:
$R_s = \rho/t = (\pi/\ln 2)V/I = 4.53V/I$ Ω-cm s >> t
Correction factor, F
Wafer thickness divided by probe spacing, W/S
Wafer diameter divided by probe spacing,
t thick compared to s
$\rho = F\rho_{measured}$
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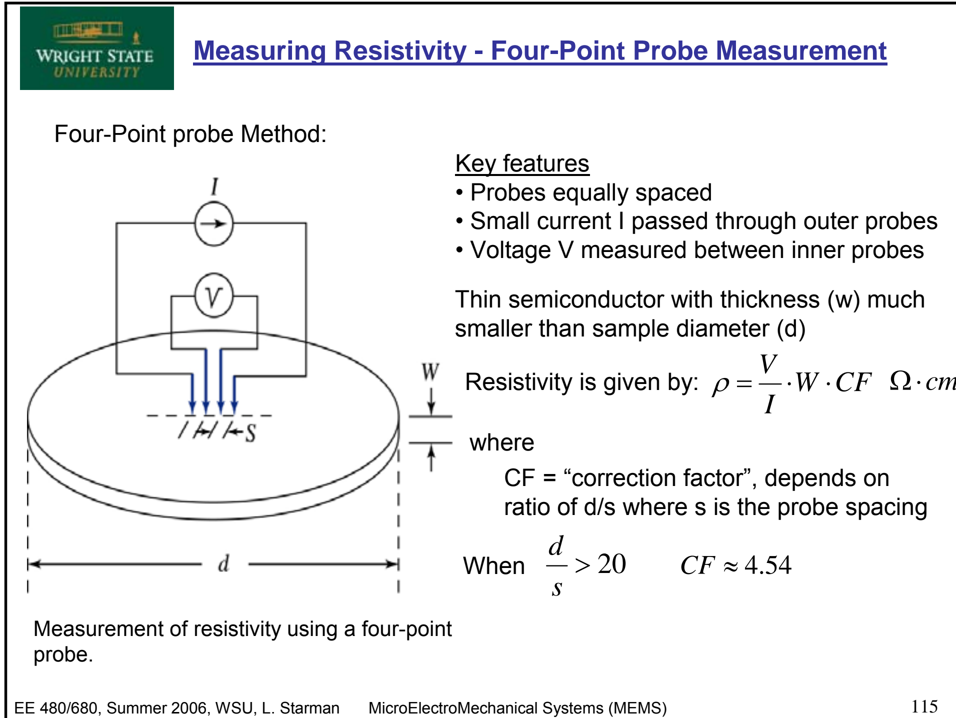
Measuring Resistivity - Four-Point Probe Measurement
WRIGHT STATE UNIVERSITY
Four-Point probe Method:
Key features
• Probes equally spaced
• Small current I passed through outer probes
• Voltage V measured between inner probes
Thin semiconductor with thickness (w) much smaller than sample diameter (d)
Resistivity is given by: $\rho = \frac{V}{I} \cdot W \cdot CF \quad \Omega \cdot cm$
where
CF = “correction factor”, depends on ratio of d/s where s is the probe spacing
When $\frac{d}{s} > 20 \qquad CF \approx 4.54$
Measurement of resistivity using a four-point probe.
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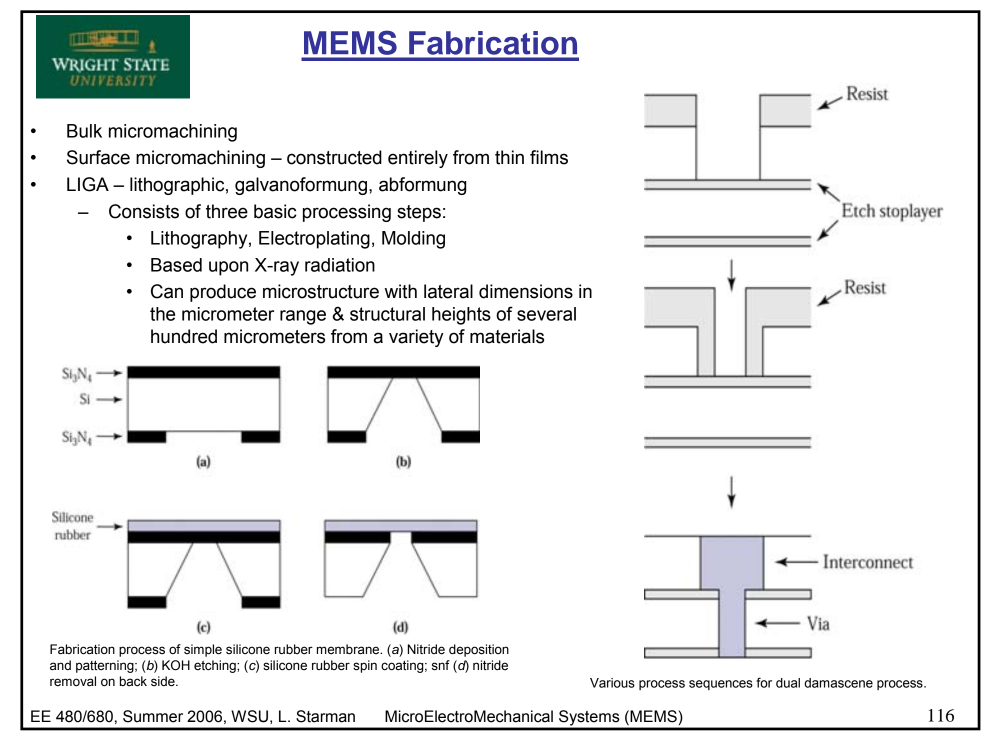
MEMS Fabrication
WRIGHT STATE UNIVERSITY
• Bulk micromachining
• Surface micromachining – constructed entirely from thin films
• LIGA – lithographic, galvanoformung, abformung
– Consists of three basic processing steps:
• Lithography, Electroplating, Molding
• Based upon X-ray radiation
• Can produce microstructure with lateral dimensions in the micrometer range & structural heights of several hundred micrometers from a variety of materials
Si_3N_4
Si
Si_3N_4
(a)
(b)
Silicone rubber
(c)
(d)
Fabrication process of simple silicone rubber membrane. (a) Nitride deposition and patterning; (b) KOH etching; (c) silicone rubber spin coating; snf (d) nitride removal on back side.
Resist
Etch stoplayer
Resist
Interconnect
Via
Various process sequences for dual damascene process.
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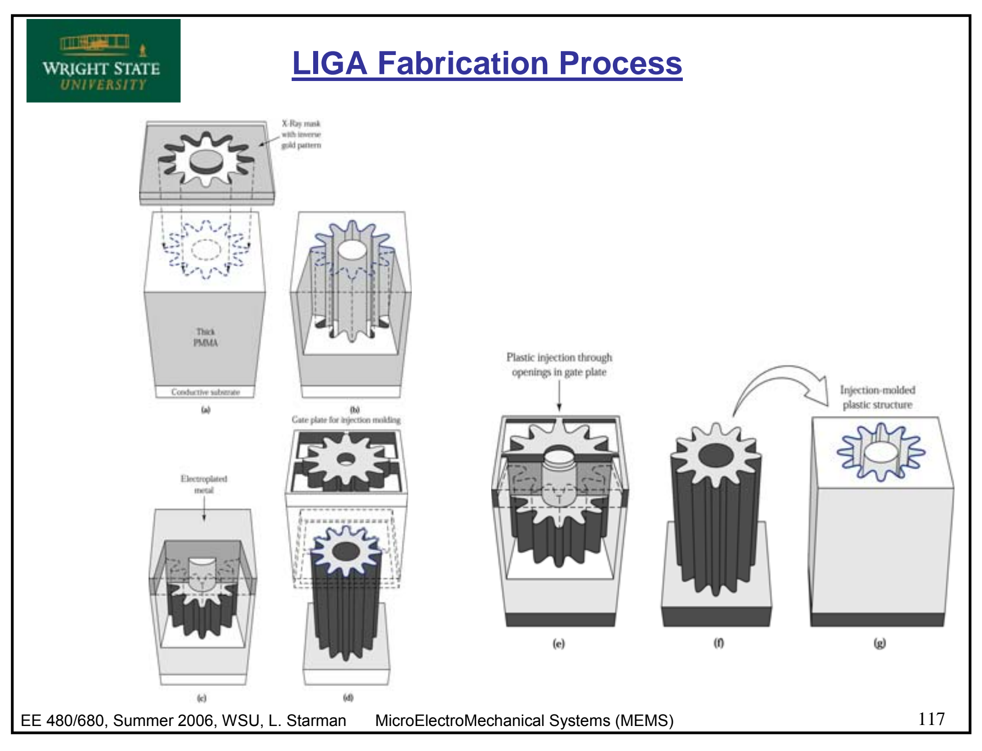
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LIGA Fabrication Process
X-Ray mask with inverse gold pattern
Thick PMMA
Conductive substrate
(a)
(b)
Gate plate for injection molding
Electroplated metal
(c)
(d)
Plastic injection through openings in gate plate
Injection-molded plastic structure
(e)
(f)
(g)
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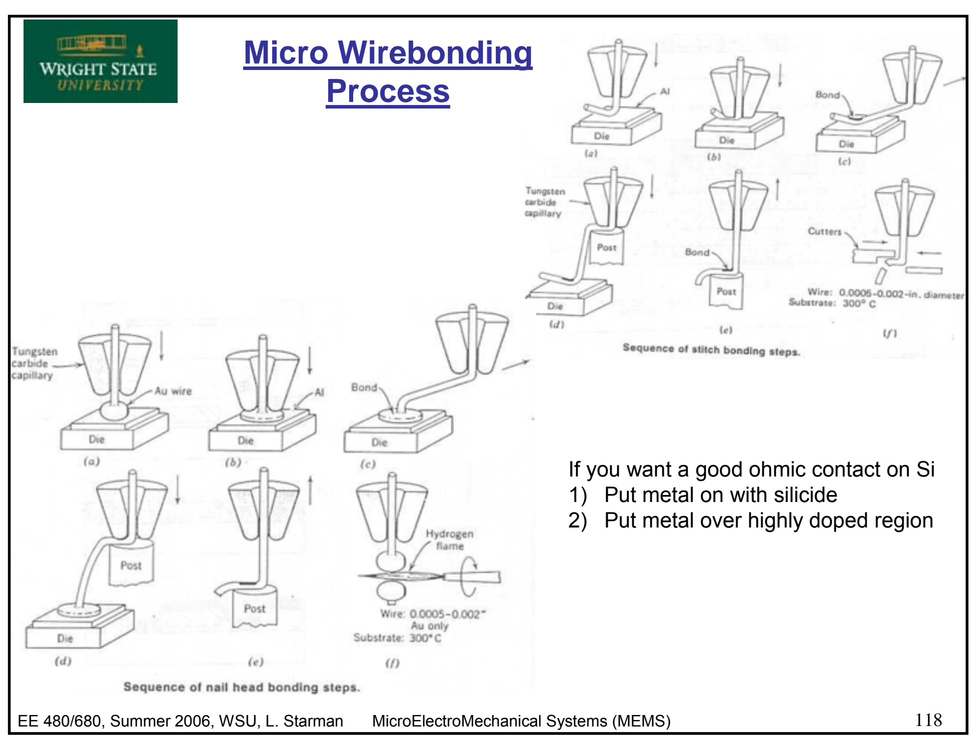
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Micro Wirebonding Process
Al
Bond
Die
(a)
(b)
(c)
Tungsten carbide capillary
Post
Bond
Cutters
Die
Post
(d)
(e)
(f)
Wire: 0.0005-0.002-in. diameter
Substrate: 300° C
Sequence of stitch bonding steps.
Tungsten carbide capillary
Au wire
Al
Bond
Die
Die
Die
(a)
(b)
(c)
Post
Post
Hydrogen flame
Die
Wire: 0.0005-0.002" Au only
Substrate: 300°C
(d)
(e)
(f)
Sequence of nail head bonding steps.
If you want a good ohmic contact on Si
1) Put metal on with silicide
2) Put metal over highly doped region
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MicroElectroMechanical Systems (MEMS)
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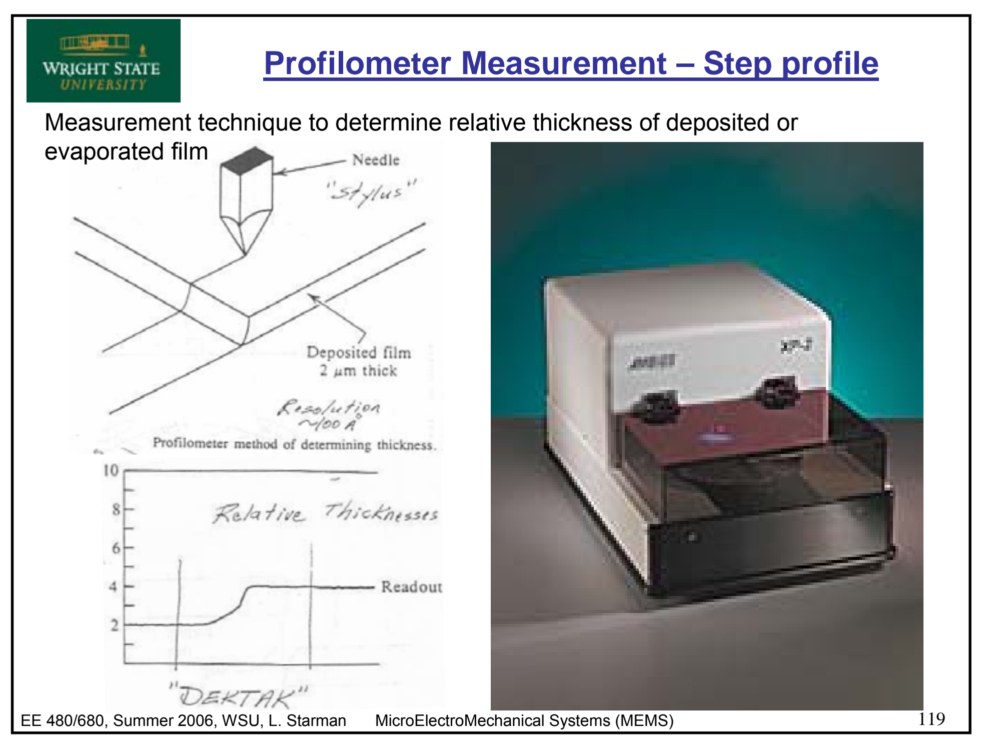

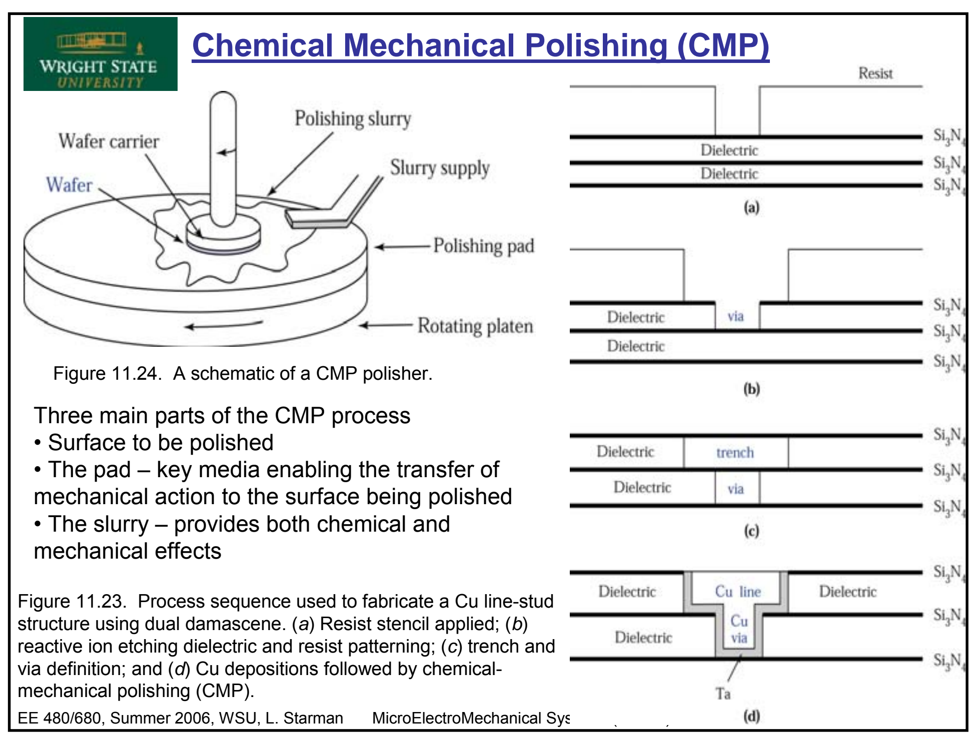

Figure 11.24. A schematic of a CMP polisher.

Figure 11.23. Process sequence used to fabricate a Cu line-stud structure using dual damascene. (*a*) Resist stencil applied; (*b*) reactive ion etching dielectric and resist patterning; (*c*) trench and via definition; and (*d*) Cu depositions followed by chemical-mechanical polishing (CMP).

Fabrication Summary

- Semiconductor Materials
- Crystal Structure
- Crystal Growth
  - Czochralski
  - Brigman
- Miller indices
- Epitaxy
- Film Formation
- Deposition
- Metalization
- Lithography
- Etching
  - Dry
  - Wet
- Doping
  - Diffusion
  - Implantation
- Resistivity
- Other useful techniques