Wright State University

EE480/680
Micro-Electro-Mechanical Systems (MEMS)
Summer 2006

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Fabrication

Spin-coating photoresist onto a wafer

MEMS Fabrication

Micromachining consists of four separate areas:

- Substrates and Dopants – Starting point
- Patterning - Lithography
- Additive Processes - Deposition
- Subtractive Process - Etching

Combining Lithography with

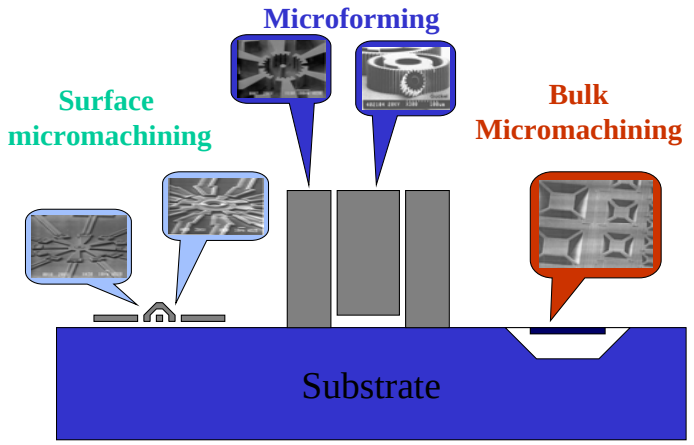
- Substrates and Dopants
- Additive Processes
- Subtractive Process

Results in Micromachining!!

MEMS Fabrication

- Micromachining combines **Lithography**, **Thin Film Processing**, and **Sacrificial Etching** to form mechanical devices
- Three Types of Fabrication Processes
  - Surface Micromachining
  - Bulk Micromachining
  - Microforming

MEMS Fabrication



Overview

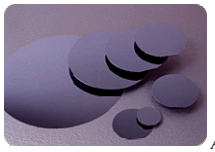
- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

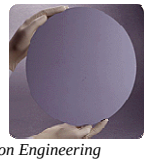
Why Silicon Processing?

1) Abundant and Inexpensive
2) Billions invested in developing pure wafers and Silicon processing
3) Native Oxide with good electrical properties

Materials

- Traditionally, MEMS have been fabricated using the same materials used in silicon (Si) based microelectronics - this is what we will concentrate on.
  - Crystalline Si
  - Polycrystalline Si (polysilicon)
  - Oxides of Si
  - Polycrystalline or Amorphous Dielectric Layers
  - Metal Films

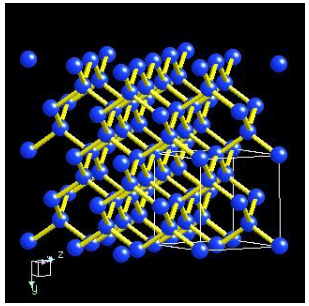


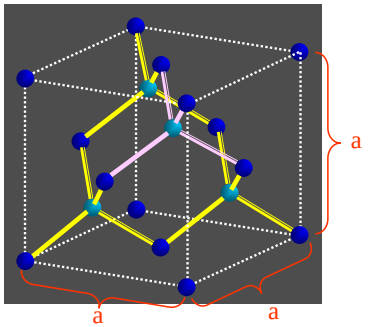


Addison Engineering

Materials

- Si crystal structure
  - Diamond, or equivalently, two interpenetrating FCC lattices by a/4 along <111>





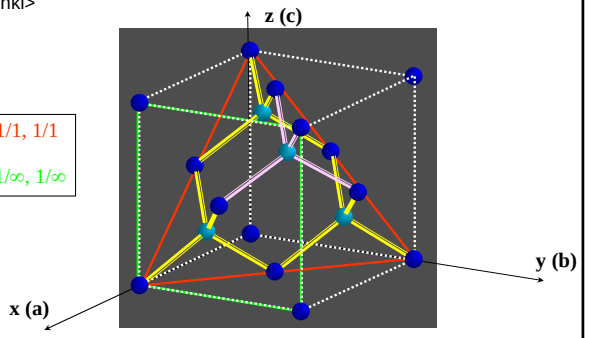
"a" is the lattice constant, for Si, a = 5.43 Å at 300 K

Materials

- Miller Indices
  - Specific plane (hkl), set of equivalent planes {hkl}
  - Specific direction [hkl] parallel to normal of plane (hkl), set of equivalent directions <hkl>

(111) = 1/1, 1/1, 1/1

(100) = 1/1, 1/∞, 1/∞



Materials: Properties

GENERAL PROPERTIES @ 300 K	Si	Ge	GaAs
Atomic Weight	28.09	72.60	144.63
Density (g/cm³)	2.328	5.3267	5.32
Atomic Density (atoms/cm³)	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Lattice Constant Å	5.43095	5.64613	5.6533
THERMAL PROPERTIES			
Melting Point (°C)	1,415	937	1,238
Specific Heat (J/g•K)	0.7	0.31	0.35
Linear Coeff. of Thermal Expansion $\alpha_L = \Delta L/(L\Delta T)$, in K^{-1})	2.6×10^{-6}	5.8×10^{-6}	6.86×10^{-6}
Thermal Conductivity (at 300 K) (W/cm•K)	1.5	0.6	0.46
Thermal Diffusivity (cm²/s)	0.9	0.36	0.24
ELECTRICAL PROPERTIES			
Energy Gap (eV) at 300 K	1.12	0.66	1.424
Intrinsic Carrier Concentration (cm^{-3})	1.45×10^{10}	2.4×10^{13}	1.79×10^{6}
Intrinsic Resistivity (Ω•cm)	2.3×10^{5}	47	10^{8}
Dielectric Constant (DC only)	11.9	16.0	13.1
* Breakdown Field (V/cm)	$\approx 3 \times 10^{5}$	$\approx 10^{5}$	$\approx 4 \times 10^{5}$
* Minority Carrier Lifetime (s)	2.5×10^{-3}	10^{-3}	$\approx 10^{-8}$
* Electron Mobility (cm²/V•s)	1,500	3,900	8,500
* Hole Mobility (cm²/V•s)	450	1,900	400

Table of basic physical, thermal, and electrical properties of Si, Ge, and GaAs. Note that the properties marked with asterisks at the left are for the highest-quality, undoped samples and are never fully achieved in practice. From Sze (1988).

Material	Yield Strength (10^9 N/m²)	Knoop Hardness (kg/mm²)	Young's Modulus (GPa)	Density (g/cm³)	Thermal Conductivity (W/cm•K)	Thermal Expansion Coefficient (10^6/K)
*Diamond	53	7,000	1,035	3.5	20	1
*SiC	21	2,480	700	3.2	3.5	3.3
*TiC	20	2,470	497	4.9	3.3	6.4
*Al_2O_3	15.4	2,100	530	4	0.5	5.4
*Si_3N_4	14	3,486	385	3.1	0.19	0.8
*Iron	12.6	400	196	7.8	0.803	12
SiO_2 (fibers)	8.4	820	73	2.5	0.014	0.55
*Si	7	850	190	2.3	1.57	2.33
Steel (max strength)	4.2	1,500	210	7.9	0.97	12
W	4	485	410	19.3	1.78	4.5
Stainless Steel	2.1	660	200	7.9	0.329	17.3
Mo	2.1	275	343	10.3	1.38	5
Al	0.17	130	70	2.7	2.36	25

Table of mechanical properties of silicon and other materials. From Petersen (1982). (Note that the values marked with asterisks at the left are for single-crystal materials and are not necessarily useful for amorphous or polycrystalline forms.)

Kovacs, *Micromachined Transducers Sourcebook*, 1998

Materials: Properties

Table 4.4 Physical properties of common non-metallic passive materials used in microsensor technology [4.15, 4.16]. Values are taken at 293 K where appropriate.

Property / Material:	Si (c)	GaAs (c)	SiO_2 (quartz)	Si_3N_4 (c)
Density, ρ_m (kg/m³)	2,330	5,316	1,544	3,440
Melting point, T_{mp} (°C)	1,410	1,510	1,880	1,900
Boiling point, T_{bp} (°C)	2,480	-	2,500	-
Thermal conductivity, κ (W/m/K)	168	47	6.5, 11	19
Specific heat capacity, c_p (J/K/kg)	678	350	730	-
Temperature expansivity, α_t (10^{-6}/K)	2.6	5.7	7, 12	0.8
Dielectric constant, ε_r	11.7	12	4.5, 4.3	7.5
Young's modulus, E (GPa)	190	-	380	380
Yield strength, Y (GPa)	6.9	-	14	14

Table 4.5 Physical properties of some common metallic passive materials used in microsensor technology [4.16].

Property: / Material:	Al	Au	Cr	Ti	W
Density, ρ_m (kg/m³)	2,699	19,320	7,194	4,508	19,254
Melting point, T_{mp} (°C)	660	1,064	1,875	1,660	3,422
Boiling point, T_{bp} (°C)	2,467	2,967	2,482	3,313	5,727
Electrical conductivity, σ (10^5 S/cm)	377	488	79	26	183
Temperature coefficient of resistance, α_r (10^{-4} /K)	43	34	30	38	-
Work function, ϕ (eV)	4.3	5.1	4.5	4.3	4.6
Thermal conductivity, κ (W/m/K)	236	319	97	22	177
Specific heat capacity, c_p (J/K/kg)	904	129	448	522	134
Linear expansivity, α_l (10^{-6} K^{-1})	23	14	4.9	8.6	4.5
Young's modulus, E (GPa)	70	78	279	~40	411
Yield strength, Y (MPa)	50	200	-	480	~750
Poisson's ratio, ν	0.35	0.44	0.21	0.36	0.28

Gardner, *Microsensors*, 1994.

Materials: Properties

Table 4.6 Some important properties of active materials used in microsensors [4.16].

	ρ_m (kg/m^3)	T_{mp} (°C)	σ (S/cm)	κ (W/m/K)	α_l (10^{-6}/K)	E_g (eV)
Thermal						
Pt	21,447	1,769	9×10^4	72	8.8	n/a
CdS	4,820	1,750	-	-	-	2.42
PbS	7,500	1,114	-	3	-	0.37
Radiation	ρ_m (kg/m^3)	T_{mp} (°C)	σ (S/cm)	κ (W/m/K)	α_l (10^{-6} /K)	E_g (eV)
Si	2,330	1,410	4×10^{-2}	168	2.6	1.11
Ge	5,323	937	3×10^{-4}	67	5.7	0.67
GaAs	5,316	1,510	10^{-8}	47	5.7	1.35
Mechanical	ρ_m (kg/m^3)	T_{mp} (°C)	Velocity (m/s)	Delay (ppm/°C)	α_l (10^{-6} /K)	K^2 (%)
Quartz (AT-cut)	1,544	1,880	5,100	2.8	0.8	1.43
Quartz (ST-cut)	1,544	1,880	4,990	33	-	1.89
$LiNbO_3$ (x-axis)	-	-	4,802	59	-	16.7
Magnetic	ρ_m (kg/m^3)	T_{mp} (°C)	σ (S/cm)	c_p (J/K/kg)	T_c (K)	μ_r (10^3)
Fe (pure)	7,874	1,535	10^5	449	1,043	1,500
NiFe alloy (50:50)	8,200	-	3×10^4	~400	798	75
CoFe alloy (50:50)	8,150	-	2×10^4	~400	1,253	7
Chemical	ρ_m (kg/m^3)	T_{mp} (°C)	σ (S/cm)	Sensitivity (ppm)	α_s (/K)	E_g (eV)
SnO_2 (c)	6,950	1,360	Low	1 - 1,000	-ve	3.45
PbPc (c)	1,950	~600	Very low	> 0.001	-ve	~0.7
Poly(pyrrole)	~1,500	~200	10^{-4}-10^{+2}	0.1 - 1,000	-ve	Small

Gardner, *Microsensors*, 1994.

Table 2.1 Properties of deposited and thermally grown oxide films (Sze 1985)

Property	Composition	Step coverage	Density ρ (g/cm^3)	Refractive index n_r	Dielectric strength (V/cm)
Thermally grown at 1000 °C	SiO_2	–	2.2	1.46	$>10^{-3}$
Deposited by $SiH_4 + O_2$ at 450 °C	$SiO_2(H)$	Nonconformal	2.1	1.44	8×10^{-6}
Deposited by TEOS at 700 °C	SiO_2	Conformal	2.2	1.46	10^{-3}
Deposited by $SiCl_2H_2 + N_2O$ at 900 °C	SiO_2	Conformal	2.2	1.46	10^{-3}

Table 2.2 Properties of some selected electronic materials

Material property	Si	GaAs	SiO_2	Si_3N_4	Al	Au	Ti
Density (kg/m^3)	2330	5316	1544	3440	2699	19 320	4508
Melting point (°C)	1410	1510	1880	1900	660	1064	1660
Electrical conductivity[a] (10^3 W^{-1} cm^{-1})	4×10^{-5}	10^{-11}	–	–	377	488	26
Thermal conductivity (W/m/K)	168	47	6.5–11	19	236	319	22
Dielectric constant	11.7	12	4.3–4.5	7.5	–	–	–
Young's modulus (GPa)	190	–	380	380	70	78	~40
Yield strength (GPa)	6.9	–	14	14	50	200	480

[a]Measured at room temperature. Some other properties will vary with temperature

Gardner, *Microsensors, MEMS and Smart Devices*, 2001.

Primary Micromachining Substrates

Elemental Semiconductors (Group IV)

- Silicon
- Germanium

Compound Semiconductors (III-V)

- Gallium Arsenide
- Indium Phosphide

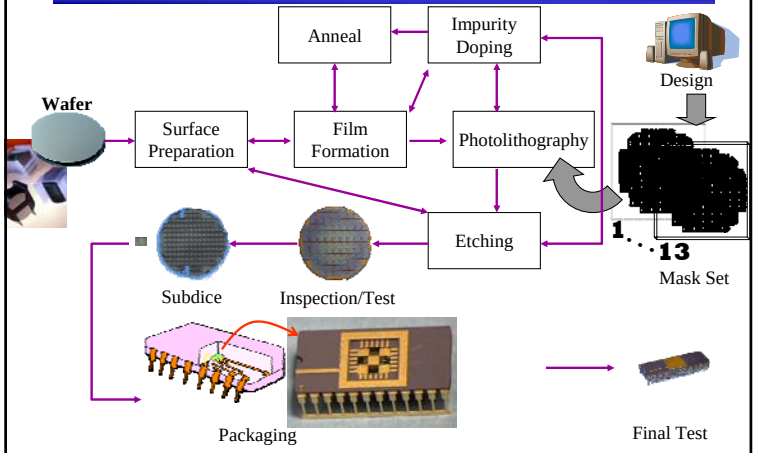
Non-Semiconductor Substrates

- Quartz
- Sapphire

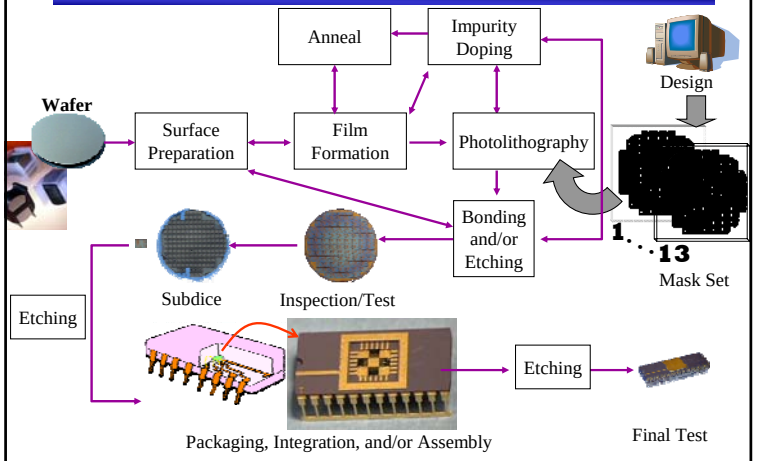
Overview

- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

Microelectronics Fabrication

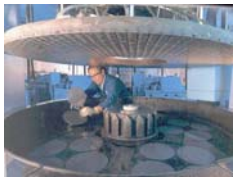


MEMS Fabrication

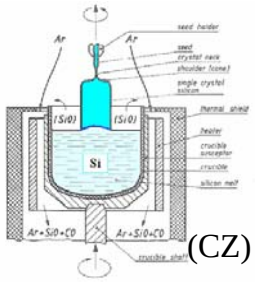


Microelectronics Fabrication

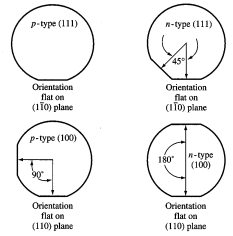
- Wafer Fabrication
  - Czochralski (CZ)
  - Float Zone (FZ)



Chemical/mechanical polishing of wafers (CMP)



(CZ)

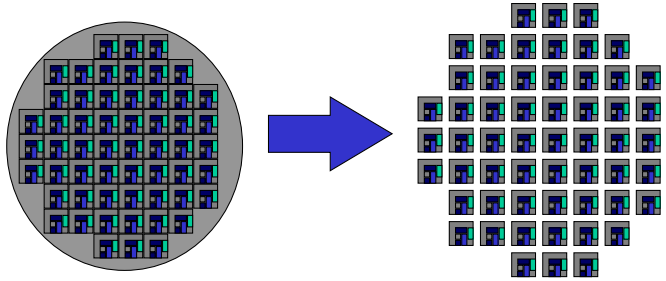


Wafer standard markings. Primary flats are shown down.

Gardner, *Microsensors, MEMS and Smart Devices*, 2001.

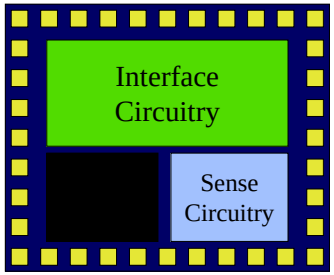
MEMS Fabrication

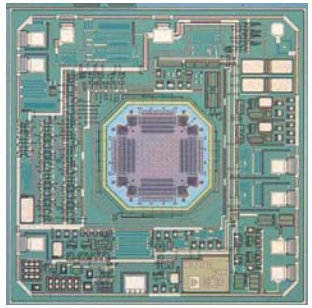
- Primarily Integrated Circuit type fabrication
  - Allows Batch Fabrication
  - Direct Sensor, Processor, Actuator Integration



MEMS Fabrication

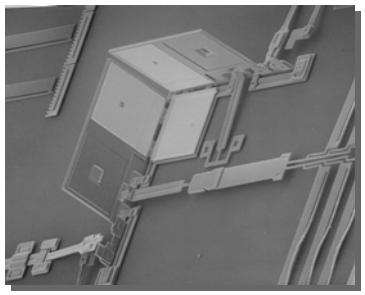
- Direct Mechanical-Electrical Integration
  - One fab process for both IC and MEMS

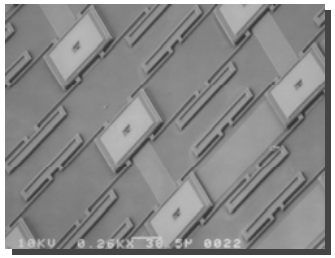




picture of ADXL202 from www.analog.com

MEMS Fabrication





Micromachining is not 3D
While a large variety of structures are possible, arbitrary 3D structures are difficult to fabricate

Microelectronics Fabrication

- Film Formation (thin < 5μm, thick < 50 μm)
  - Thermal Oxidation (wet/dry)
    - The enhancement of the transformation of Si into SiO_2, consumption ratio 0.44 Si/SiO_2
    - Amorphous thin films, conformal coating
    - 1000 - 1200 °C, atmospheric pressure, hours deposition times
    - Passivation, sacrificial layers, hard etch/diffusion mask, insulation
  - Chemical Vapor Deposition (CVD)
    - LPCVD, MOCVD, PCVD
    - The nucleation of a gaseous species on a substrate to form a film
    - Polycrystalline or Amorphous thin films, conformal coating
    - ≈ 600 °C, low - atmospheric pressure, on order of 1 μm/hour deposition rates
    - Structural layers, passivation, sacrificial layers, hard etch/diffusion mask, insulation, some metals, SiO_2, Si_3N_4, polySi, phosphosilicate glass (PSG)

Microelectronics Fabrication

- Film Formation (thin < 5μm, thick < 50 μm)
  - Evaporation
    - The evaporation of metals by resistive, inductive, or electron beam heating in order for condensation to occur on a substrate, thereby, forming a film
    - Amorphous thin films, semi-conformal coating
    - From melting temperature of metal to 200 °C, high vacuum, on order of 2 μm/hour deposition rates
    - Metal conductor lines, solder deposition, mirror surfaces, electrical contacts

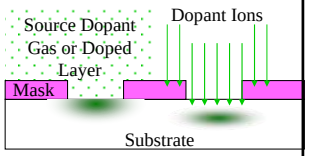
Microelectronics Fabrication

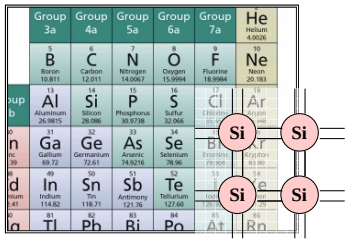
- Film Formation (thin < 5μm, thick < 50 μm)
  - Sputtering
    - The physical removal of atoms from a target by energized ions (plasma) and reformation of a film on a substrate
    - Amorphous thin films, conformal/nonconformal coatings
    - High vaccum
    - Most materials can be sputtered: metals, organics, inorganics
  - Electroplating
    - The electrochemical reaction of a solution, on a seed surface, to form a metal film
    - Amorphous thick and greater films
  - Spin Casting
    - Thin film material dissolved in a volatile liquid solvent, spin coated onto a substrate to form films
    - Low quality, but convenient amorphous thin or thick films
    - Room temperature application, ≈ 100 °C cure temperatures
    - Organic polymers, inorganic glasses

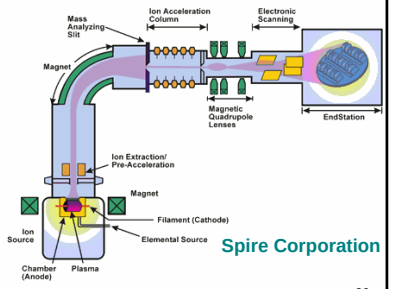
Sputtering System

Microelectronics Fabrication

- Impurity Doping
  - Si or polysilicon doped for the purpose of increasing conductivity or creating etch stops
  - Constant/Limited Source Diffusion or Ion Implantation
  - B in Si is p-type
  - P in Si is n-type







Spire Corporation

Microelectronics Fabrication

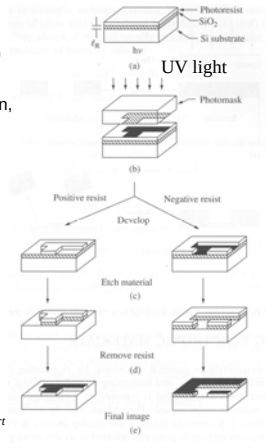
- Photolithography
  - The technique of transferring a pattern to a surface
    - Etch masks (soft), insulating layers, passivation, protection, structures
    - Contact, Proximity, and Printing

Table 2.3 Some properties of the common spin-on materials

Material	Thickness (μm)	Bake temperature (°C)	Solvent
Photoresist	0.1–10	90–150	Weak base
Polyimide	0.3–100	350–450	Weak base
Silicon dioxide	0.1–0.5	500–900	HF
Lead titanate	0.1–0.3	650	HNO_3

Table 2.4 Commercially available resists

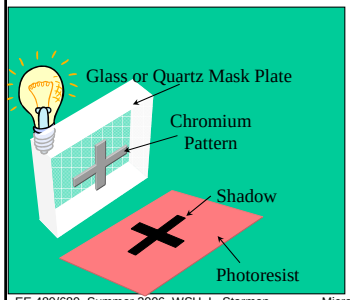
Resist	Lithography	Type
Kodak 747	Optical	Negative
AZ-1350J	Optical	Positive
PR102	Optical	Positive
Poly(methyl methacrylate) (PMMA)	E-beam and X ray	Positive
Poly[(glycidyl methacrylate)-co-ethylacrylate] (COP)	E-beam and X ray	Negative
Dichloropropyl acrylate and glycidyl methacrylate-co-ethyl acrylate (DCOPA)	X ray	Negative

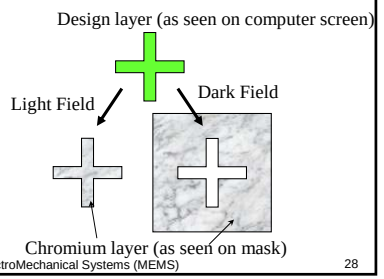


Gardner, *Microsensors, MEMS and Smart Devices*, 2001.

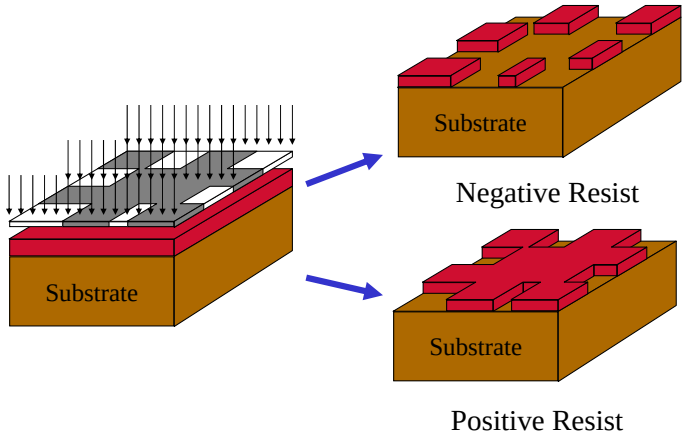
Microelectronics Fabrication

- Photolithography - Mask Production
  - When masks are designed, each design layer must be specified as either:
    - **Light Field** or **Dark Field**
    - With light field, a polygon on your design will appear as a polygon of chrome (which will block UV) on the mask. Conversely for dark field.
    - The type of photoresist (positive or negative) will determine what the developed features look like.





Lithography



Microelectronics Fabrication

- Photolithography

Spinner Bench and Relevant Chemicals & Supplies

Mask Aligner

Microelectronics Fabrication

- Etching
  - The process of selectively removing material
    - Wet, Gas, Plasma Assisted (RIE)

Wet Bench

Nippon Scientific Co., Ltd
Reactive Ion Etcher

Microelectronics Fabrication

- Etching

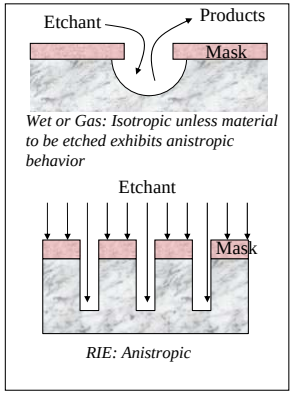


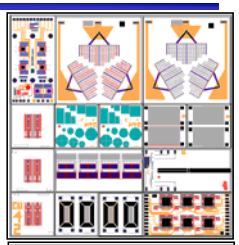
Table 2.5 Wet etchants used in etching some selected electronic materials

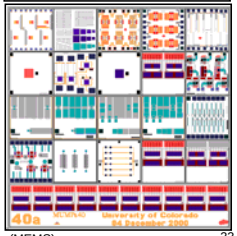
Material	Etchant composition	Etch rate (Å/min)
Si	3 ml HF + 5 ml HNO_3	3.5×10^5
GaAs	8 ml H_2SO_4 + 1 ml H_2O_2 + 1 ml H_2O	0.8×10^5
SiO_2	28 ml HF + 170 ml H_2O + 113 g NH_4F	1000
	or	
	15 ml HF + 10 ml HNO_3 + 300 ml H_2O	120
Si_3N_4	Buffered HF or H_3PO_4	5 or 100
Al	1 ml HNO_3 + 4 ml CH_3COOH + 4 ml H_3PO_4 + 1 ml H_2O	350
Au	4 g KI + 1 g I_2 + 40 ml H_2O	1.0×10^5

Gardner, *Microsensors, MEMS and Smart Devices*, 2001.

Microelectronics Fabrication: Dicing

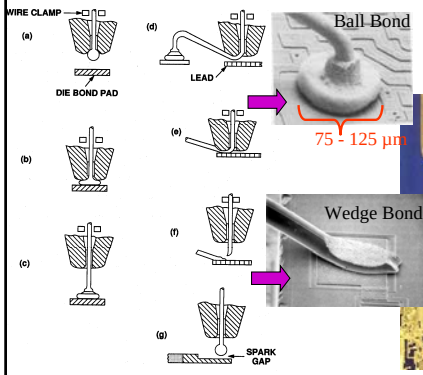
- Precision slices of semiconductor or ceramic wafers
  - 100 μm wide cuts in Si with a diamond blade

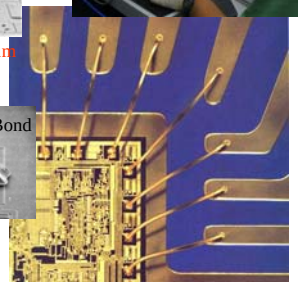




Microelectronics Fabrication: Wire Bonding

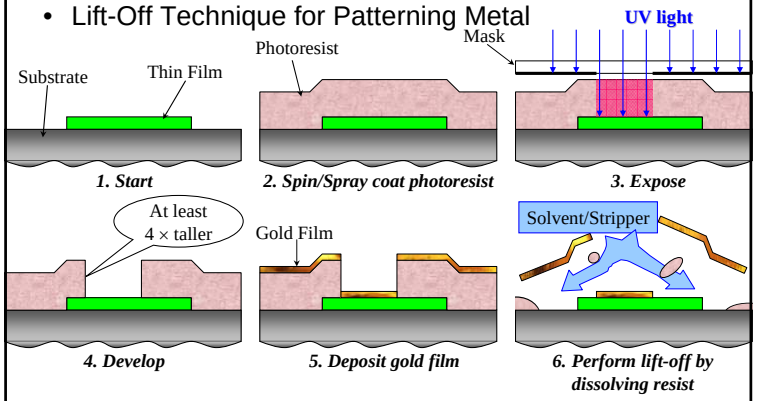
- To connect electrical contacts on chip to package or other chips
  - Gold or Aluminum wires 25 μm in diameter





Microelectronics Fabrication

- Lift-Off Technique for Patterning Metal



Overview

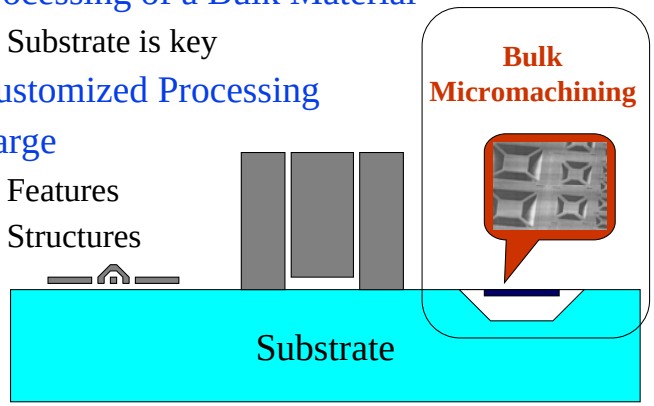
- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

Bulk Micromachining: Si

- A Subtractive Process
  - Beginning with a Si substrate, Si is removed from the bulk of the substrate, using etching, to form features.

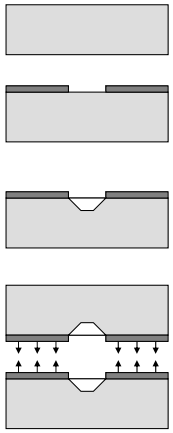
Bulk Micromachining

- Processing of a Bulk Material
  - Substrate is key
- Customized Processing
- Large
  - Features
  - Structures



Bulk Micromachining Topics

- Substrates
- Masking
  - Thin Film Processing
- Etching
  - Removing Undesired Material
- Wafer Bonding
  - Adding Additional Material



Primary Micromachining Substrates

Elemental Semiconductors (Group IV)
- Silicon
- Germanium

Compound Semiconductors (III-V)
- Gallium Arsenide
- Indium Phosphide

Non-Semiconductor Substrates
- Quartz

Why Silicon Processing?

1) Abundant and Inexpensive
2) Billions invested in developing pure wafers and Silicon processing
3) Native Oxide with good electrical properties

Bulk Substrate Advantages

Purity
- High quality substrates are readily available and relatively inexpensive

Material Properties
- Mechanical and electrical properties are typically well known
- Properties are more uniform than thin film properties
- Fewer issues with internal stresses

Structure
- Typically well known

Masking

- Masking is the process of protecting the substrate for a following etch process
- Standard thin film techniques
- Ideal mask properties
  - Easy to deposit and pattern
  - Non reactive - particularly to the bulk etchant
  - Easily removed
- Typical Films Used Include
  - SiO_2
  - Si_xN_y
- Why not Photoresist?
- Standard IC Issues
- MEMS related issues
  - Selectivity
  - Mask thickness
  - Two sided processing
  - Non-planar surfaces
  - IC Compatibility

Mechanical Properties

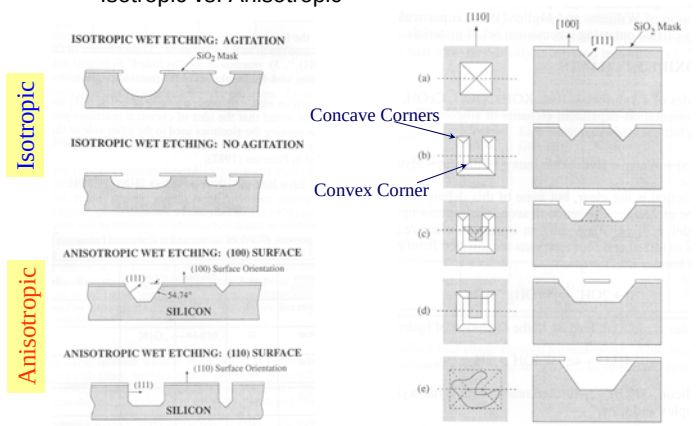
	Yield Strength (10^{10} dyne/cm^2)	Knoop Hardness (kg/mm^2)	Young's Modulus (10^{12} dyne/cm^2)	Density (gr/cm^3)	Thermal Conductivity (W/cm°C)	Thermal Expansion (10^{-6}/°C)
*Diamond	53	7000	10.35	3.5	20	1.0
*SiC	21	2480	7.0	3.2	3.5	3.3
*TiC	20	2470	4.97	4.9	3.3	6.4
*Al_2O_3	15.4	2100	5.3	4.0	0.5	5.4
*Si_3N_4	14	3486	3.85	3.1	0.19	0.8
*Iron	12.6	400	1.96	7.8	0.803	12
SiO_2 (fibers)	8.4	820	0.73	2.5	0.014	0.55
*Si	**7.0**	**850**	**1.9**	**2.3**	**1.57**	**2.33**
Steel	4.2	1500	2.1	7.9	0.97	12
W	4.0	485	4.1	79.3	1.78	4.5
Stainless Steel	2.1	660	2.0	7.9	0.329	17.3
Mo	2.1	275	3.43	10.3	1.38	5.0
Al	0.17	130	0.70	2.7	2.36	25

*single crystal.

(From "Silicon as a Mechanical Material," K.E. Petersen, Proc. of the IEEE, Vol. 70, No. 5, pp. 420-457, May 1982.)

Bulk Micromachining: Si

- Isotropic vs. Anisotropic

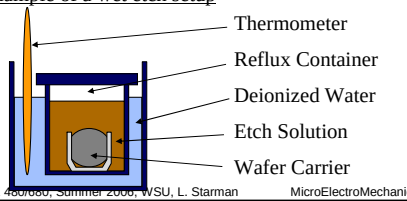


Etching

Etching is the process of removing a material. The key to making etching useful is to precisely and repeatably control the material that is removed.

Types of Etches
- Environment
  - Wet
  - Dry
  - Plasma
- Mechanism
  - Physical
  - Chemical

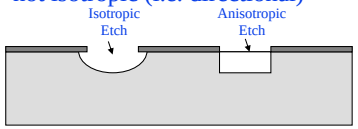
Example of a wet etch setup



Example wet bench picture from: http://www.vinylglass.com/instant.shtml

Etch Directivity

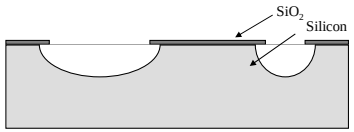
- Isotropic - Non-directional
- Anisotropic - not isotropic (i.e. directional)



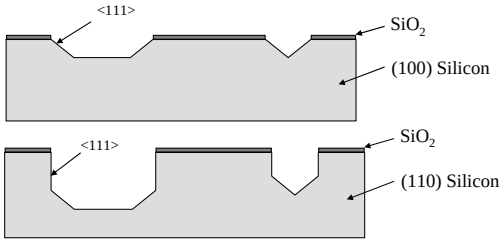
To date, the majority of MEMS processing has been done with the wet bulk etching of silicon. This is primarily due to availability of the substrate materials and chemicals. Recent work has been looking at two promising etch processes: deep RIE and xenon difluoride etching

Wet Isotropic Etching

- Etch proceeds nearly equally in all directions
- Primarily a diffusion limited process
- Most common etchant:
  "HNA" = HF/HNO_3/Acetic Acid : 10/30/80

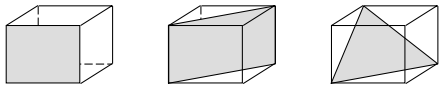


Wet Anisotropic Etching



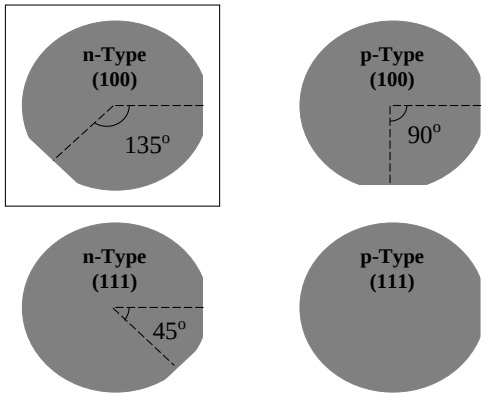
- Etch rate varies with the etch direction
- Typically determined by the crystal planes

Miller Indices



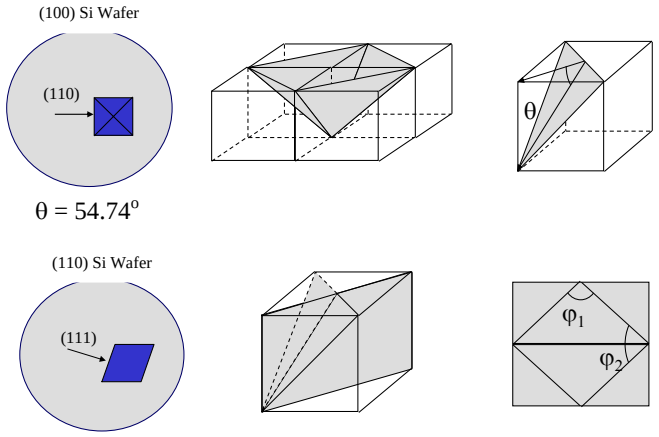
(100) (110) (111)

SEMI Standard Wafer Flats

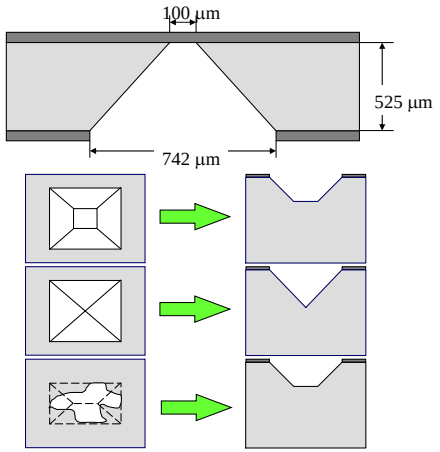


The primary flat is specified to be the (110) crystal plane

Anisotropic Etching

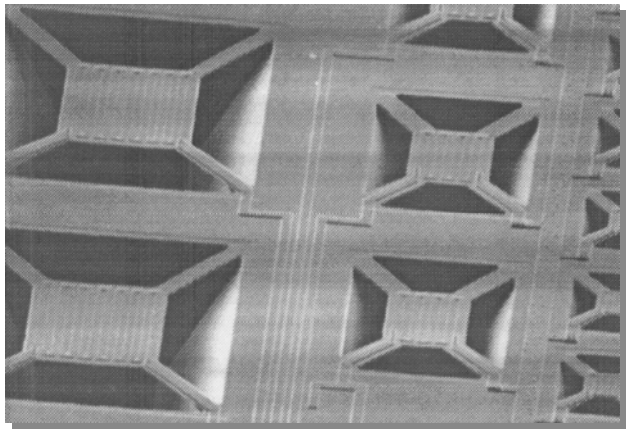


Wet Anisotropic Etching



- Etching a 100 micron wide via through a 525 micron wafer requires an opening that is 742 microns wide

Suspended Structures



Anisotropic Etching

- Primary Etchants
  - Alkali hydroxyls (KOH)
  - EDP
  - Quaternary ammonium hydroxides (TMAH)
- Choice of etchant depends on:
  - Etch Rate
  - (100)/(111) Etch Ratio
  - Hillock formation
- Potassium Hydroxide (KOH)
  - High Etch Rate
  - Good Masking Selectivity
  - Excellent (110) to (111) Etch Selectivity
- 50% By Wt. at 85 deg. C
  - 2.0 μm/min (110)
  - > 200:1 selectivity for (110) SiO_2
  - > 250:1 selectivity for (110):(111)
  - (110):(111) selectivity depends on alignment

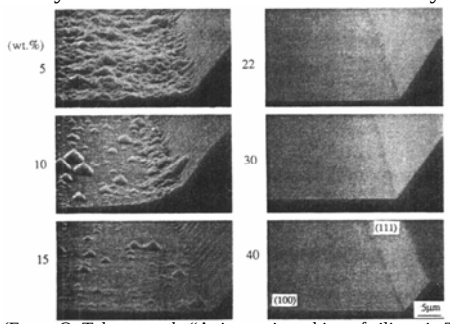
Potassium Hydroxide (KOH)

Formulation	Temp. (°C)	Etch Rate (μm/min)	(100)/(111) Etch Ratio	Masking Films (etch rate)
KOH (44 g) Water, Isopropanol (100 ml)	85	1.4	400:1	SiO_2 (1.4 nm/min) Si_3N_4 (negligible)
KOH (50 g) Water, Isopropanol (100 ml)	50	1.0	400:1	Same as above
KOH (10 g) Water, Isopropanol (100 ml)	65	0.25 - 1.0	-	SiO_2 (0.7 nm/min) Si_3N_4 (negligible)

- Ethylene diamine Pyrocatechol (EDP)
  - EDP (750 ml)
  - Pyrocatechol (120 g)
  - Water (100 ml)
- At 115 °C
  - 0.75 μm/min (100)
  - 35:1 (100)/(110) Etch Ratio
- TetraMethyl Ammonium Hydroxide (TMAH)
  - Wide Availability
  - Excellent Masking Selectivity (> 1000/1)
  - Al selectivity varies with solution ph
- 22% by wt. TMAH in DIW at 90 °C
  - approx. 1.0 μm/min
  - approx. 25/1 (100)/(111) etch ratio

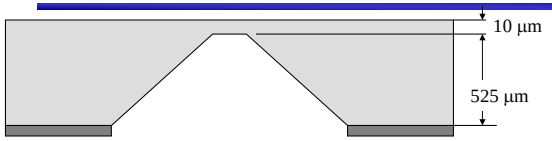
Anisotropic Etching

- Hillock Formation
  - Results from hydrogen bubbles
  - Generally a function of etch rate and selectivity



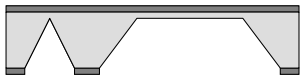
(From: O. Tabata, *et al*., "Anisotropic etching of silicon in TMAH solutions", *Sensors and Actuators A*, vol. 34, pp. 51-57, 1992.

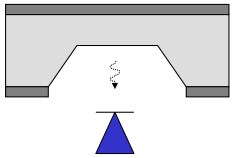
Wet Anisotropic Etching



- Precision depth control is difficult to achieve
- Three techniques are common:
  - Timed Etches
  - IR Absorption
  - Etch cavities

IR Radiation

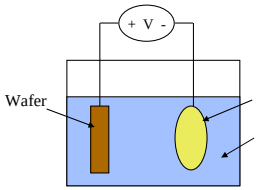


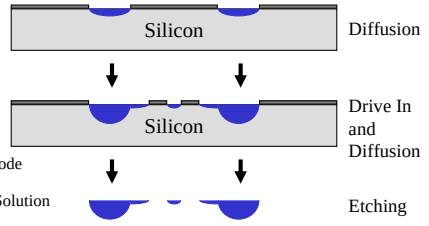


Dopant Dependent

- Electrochemical Etching (ECE)
  - Etch rate controlled by electrical potential
- Dopant Dependent
  - Etch rate is modulated by wafer doping

ECE





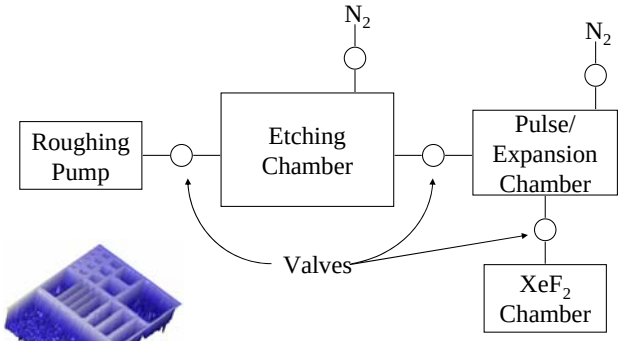
Dry Etching

- Vapor Phase Etching
  - XeF_2
- Plasma Etching
  - Deep RIE

Why XeF_2?

- Provides a non-plasma isotropic dry etch
- Excellent selectivity for CMOS materials
- Excellent Photoresist selectivity
- Simple System Set Up
- Good Etch Rate

XeF_2 Etching

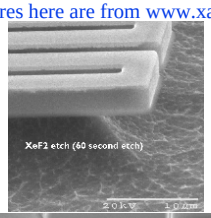


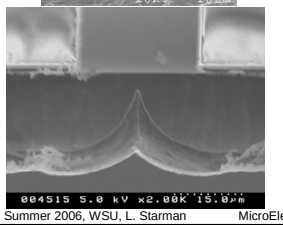
3D Profile of silicon etched using XeF_2

$$2\ XeF_2 + Si \Rightarrow Xe + SiF_4$$

XeF_2 Etching

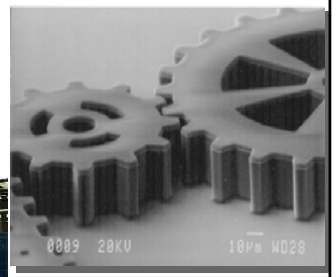
- Commercial Systems are now available
  - Pictures here are from www.xactix.com





Deep RIE

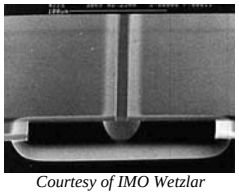
- Modified from standard reactive ion etching
- Allows vertical side walls on (100) wafers
- Good Etch Profiles
  - Etching up to 1 mm deep
- Masking with photoresist
- IC Process Compatible
- 200:1 Aspect Ratios
- Also done with GaAs



Picture of the Stanford Nanotechnolgy Centers ICP RIE system

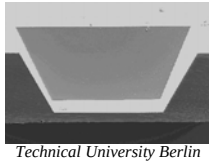
http://snf.stanford.edu/Equipment/stsetch/stsetch2.jpg

Bulk Micromachining: Si Etchants



Courtesy of IMO Wetzlar

isotropic
RIE
note: RIE is mainly used for its anisotropy



Technical University Berlin

anisotropic
KOH †
(an Alkali Hydroxide)

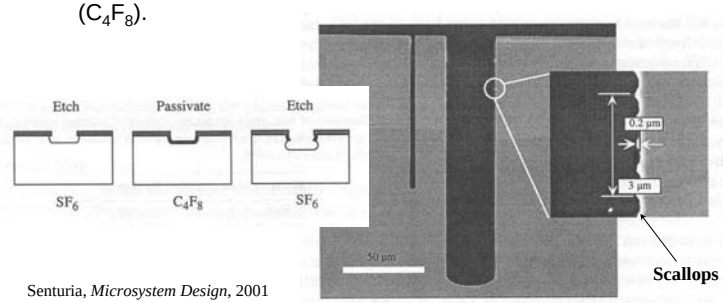
Comparison of Example Silicon Etchants

	HNA (HF+HNO_3 +Acetic Acid)	† Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide)	XeF_2	SF_6 Plasma	DRIE (Deep Reactive Ion Etch)
Etch Type	wet	wet	wet	wet	dry [1]	dry	dry
Anisotropic?	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Si Etch Rate μm/min	1 to 3	1 to 2	1 to 30	~ 1	1 to 3	~ 1	> 1
Si Roughness	low	low	low	variable[2]	high [3]	variable	low
Nitride Etch	low	low	low	1 to 10 nm/min	?	low	low
Oxide Etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	~ 1 nm/min	low	low	low
Al Selective	no	no	no [4]	yes [5]	yes	yes	yes
Au Selective	likely	yes	yes	yes	yes	yes	yes
p++ Etch Stop?	no (n slows)	yes	yes	yes	no	no (some dopant effects)	no
Electrochemical Stop?	?	yes	yes	yes	no	no	no
CMOS Compatible? [6]	no	no	yes	yes	yes	yes	yes
Cost [7]	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate?	high	high

1 Sublimation from solid source.
2 Varies with wt% TMAH, can be controlled to yield very low roughness.
3 Addition of Xe to vary stoichiometry in F or Br etch systems can yield optically smooth surfaces.
4 Some formulations do not attack Al, but are not common.
5 With added Si, polysilicic acid or pH control.
6 Defined as 1) allowing wafer to be immersed directly with no special measures and 2) no alkali ions.
7 Includes cost of equipment.

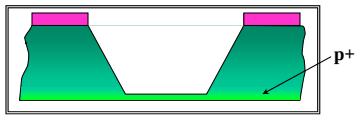
Bulk Micromachining: Si Etchants

- Deep Reactive Ion Etch DRIE
  - Alternating steps of etching (SF_6) and polymer formation (C_4F_8).

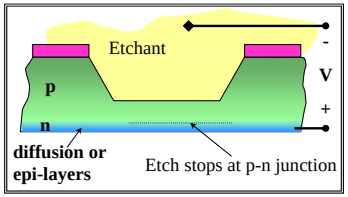


Senturia, *Microsystem Design*, 2001

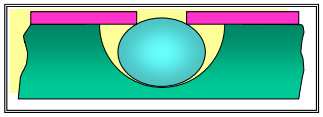
Bulk Micromachining: Etch Stops



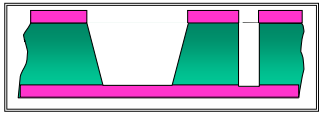
- Crystallographic
  - (111) stop
- Doping
  - p+ (Boron) stops the etch "p-stop"



- Electrochemical
  - Higher potential relative to etchant promotes oxide growth
  - "Junction-stop"



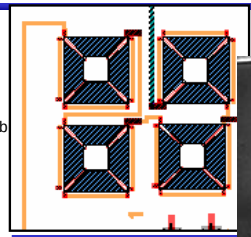
- Reactant Limited
  - Reaction products form bubble that blocks arrival of reactants



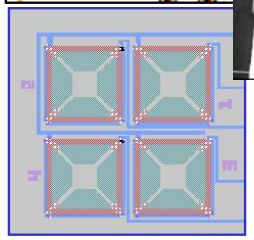
- Dielectric Film Stop

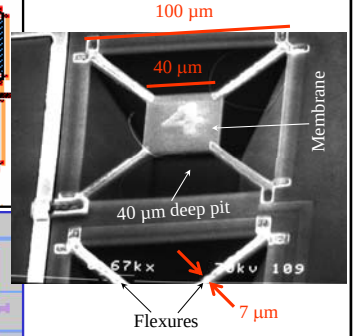
Bulk Micromachining: Case Study

- A post-processing step after MEMS fab



- A post-processing step after microeletronics fab





Layouts and SEM courtesy of Li-Anne Liew, 2001

Bulk Micromachining: Case Study

- A custom process step: Motorola MPX4080D series piezoresistive differential pressure sensor

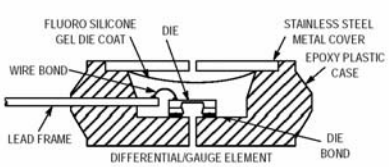
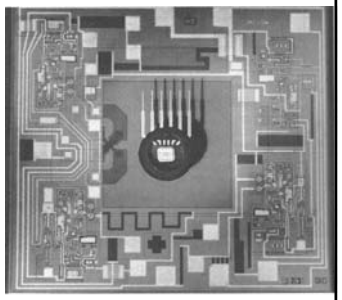


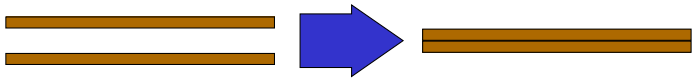
Figure 3. Cross–Sectional Diagrams (Not to Scale)



Wafer Bonding

- Used to create high-aspect ratio: multilayer structures, sealed cavities, multilevel chambers, etc.
- Anodic Bonding
  - Glass to Si or SiO_2
    - 0.5 μm metal lines can pass under seal
    - 1.2 kV @ 400 °C, + (anode) on Si
  - Si to deposited glass on Si substrate
    - 30 - 60 V @ 400 °C, + (anode) on Si
- Fusion Bonding
  - Si to Si with or "without" SiO_2
  - Clean wafers at ≈ 800 °C
- Other Low Temperature Methods
  - Temperature limit for IC processed standard substrates is 450 °C

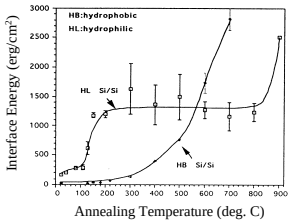
Wafer Bonding



- The permanent joining of two substrates
  - Covalent bonding
  - Glue layer
- Widely applicable to Micromachining
  - Buried layers
  - Packaging
- Silicon Fusion Bonding
  - Si-Si, Si-O-Si
- Anodic Bonding
  - Electrostatic Force
  - Si-Glass
- Low Temperature Melting Glass
  - Si-Glass-Si
- Metal Bonding

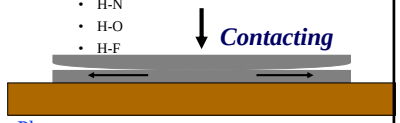
Fusion Bonding

- Three Basic Steps
  - Surface Preparation
    - Flat
    - Roughness less than 0.5 nm
    - Hydrophilic *
  - Contacting
    - Immediately after preparation
  - Annealing
    - Bond Depends on Temperature



Surface Preparation

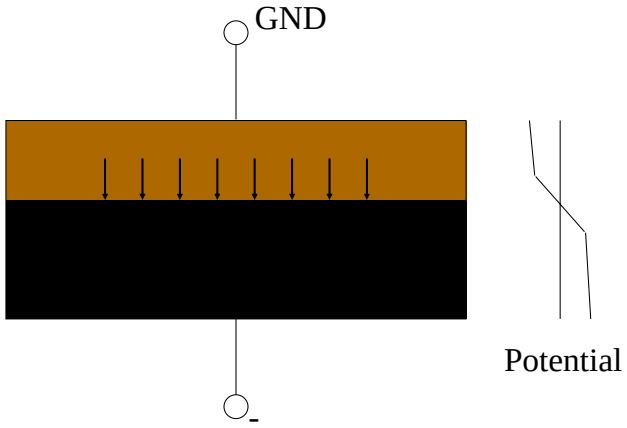
- Residue Free Organic Etch
  - Sulfuric Acid
  - Acetone/Methyl
  - Boiling Nitric Acid Solutions
- Hydrophilic vs. Hydrophobic
- RT bonding is due to Hydrogen bonding
  - H-N
  - H-O
  - H-F



- Three Phases
  - Below 300 deg. C
  - 300-800 deg. C ← ***Annealing***
  - Above 800 deg. C

Excerpted from: "Semiconductor wafer bonding: recent developments," Materials Chemistry and Physics, 37 (1994), pp. 101-127.

Anodic Bonding



Anodic Bonding

EV Group EVG 501 manual bonder
www.evgroup.com
Temp: up to 550 °C
Force: up to 3400N (765 lbf)
Opt. to 7000 N
Alignment: +/- 5 μm
Max. Field: 1.2 kV (2kV opt.)
Wafer size: up to 6 in dia.
Pressure: 1E-5 mBarr – 2 Barr

EV Group Gemini production bonder

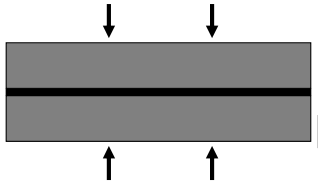
Anodic Bonding

AML Wafer Bonder AML-402
www.aml.co.uk
Temp: up to 560 °C
Force: up to 2000N (450 lbf)
Alignment: +/- 5 μm
Max. Field: 2.5 kV
Wafer size: up to 6 in dia.
Chamber Pressure: 1E-5 mBarr - ?

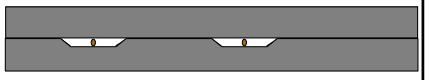
Anodic Bonding

- Low bonding temperature giving more design flexibility (300-500 C)
- Thermally matched stress free bond
- No measurable flow of the glass occurs
- Since glass is an electrical insulator, parasitic capacitances are kept extremely small
- Hermetic seals.
- High strength bond - higher than the fracture strength of glass

Low Melting Point Glass
High Pressure and Temperature

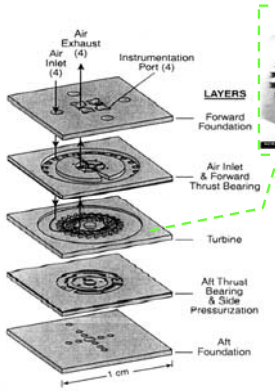


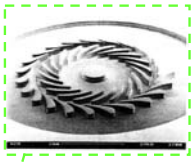
- Primary Problems
  - Thermal Mismatch
  - Dirty Surfaces
    - 1 μm particle -> 5 mm unbonded region



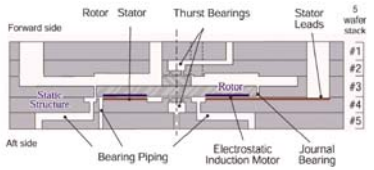
Bulk Micromachining and Bonding: Case Study

- MIT micro shirt-button-sized turbine:





A. H. Epstein, et al., "Shirtbutton-Sized Gas Turbines: The engineering Challenges of Micro High Speed Rotating Machinery," Symp. on Transport Phenomena and Dynamics of Rotating Machinery, March 2000.



L. G. Fréchette, et al., "An Electrostatic Induction Micromotor Supported On Gas-lubricated Bearings," *MEMS 2001*

Wafer Bonding Example

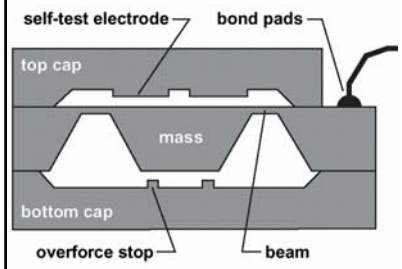


Figure 2. Cross-sectional View of Accelerometer Die

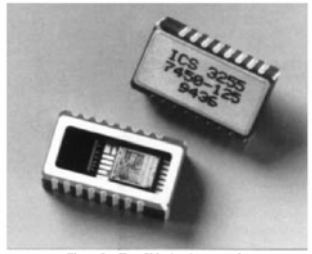
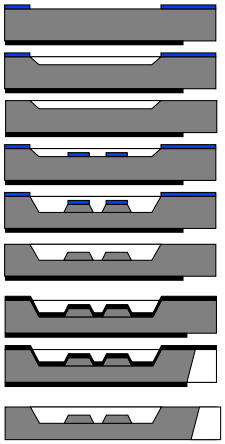


Figure 1. Two Chip Accelerometer in Hermetically Sealed Package

Figures from: "An Inertial-Grade, Micromachined Vibrating Beam Accelerometer", IC Sensors white paper

Wafer Bonding Example



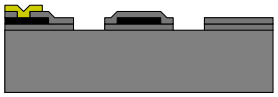
Notional process – Cap wafers

1. Deposit and pattern masks – silicon oxide on front, nitride on back
2. Bulk Etch (KOH)
3. Mask Strip
4. Deposit and pattern 2nd mask
5. Bulk Etch
6. Mask Strip

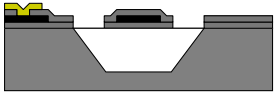
Notional process – Bottom wafer

1. Protect front with thick resist (spray on)
2. Bulk Etch (KOH)
3. Strip Resist and Back side mask

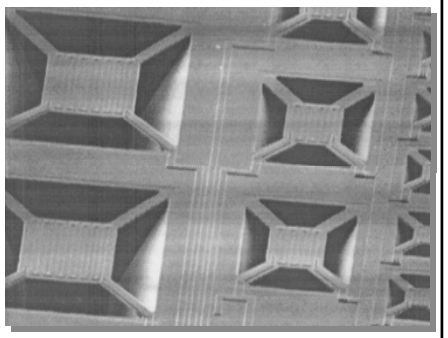
CMOS Post Processing



Standard IC process – But all oxide cuts are aligned to expose bare silicon in some regions



After IC fabrication is complete, a bulk silicon etch is performed



Overview

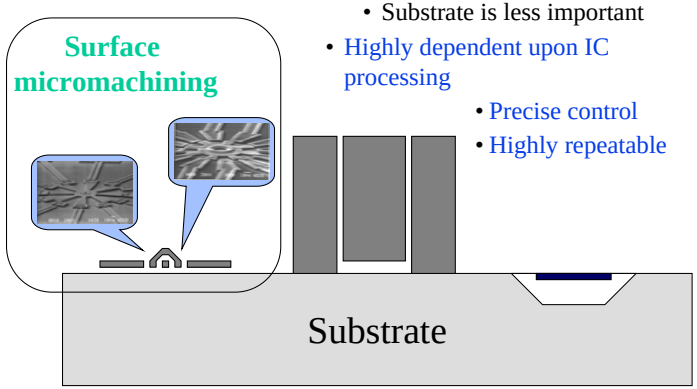
- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

Surface Micromachining

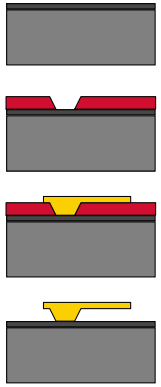
- An Additive Process
  - Beginning with a substrate, thin films are deposited on top of the substrate and patterned, using etching, to form features.
  - Structural layers are separated by “sacrificial layers” which are removed at the end of the fabrication process.

MEMS Fabrication

- Building on top of the substrate
  - Substrate is less important
- Highly dependent upon IC processing
  - Precise control
  - Highly repeatable



Surface Micromachining



1) Deposit A Passivation Layer

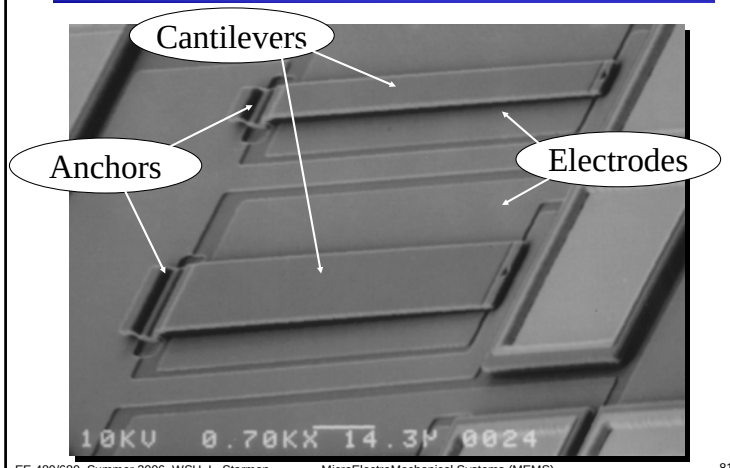
2) Deposit and Pattern the Sacrificial Layer

3) Deposit and Pattern the Structural Layer

4) Remove the Sacrificial Layer

Structural Layer (Au)
Sacrificial Layer (Polyimide)
Passivation Layer (Nitride)
Substrate (Silicon)

Surface Micromachining

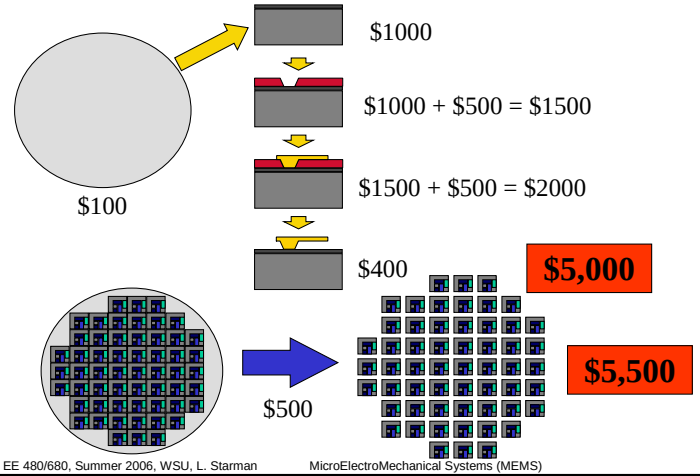


Surface Micromachining

Structural Layers	Sacrificial Layers
Si_3N_4	SiO_2, Photoresist
Al, SiO_2	Polysilicon
Polysilicon	SiO_2
Al	Photoresist
Polyimide	Al

Note, many of the sacrificial layers are used in the design of IC's

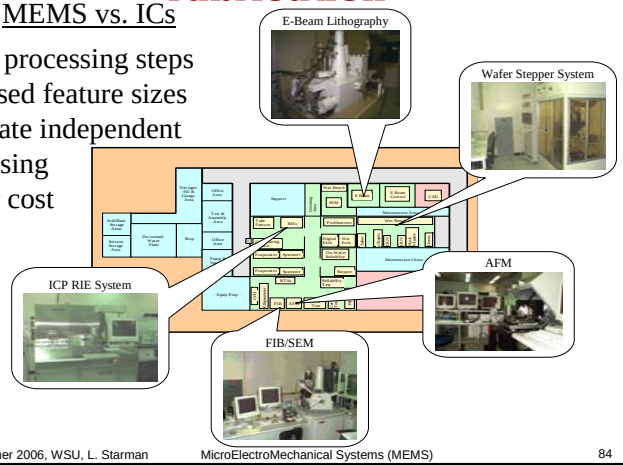
Surface Micromachining



Surface Micromachining Fabrication

MEMS vs. ICs

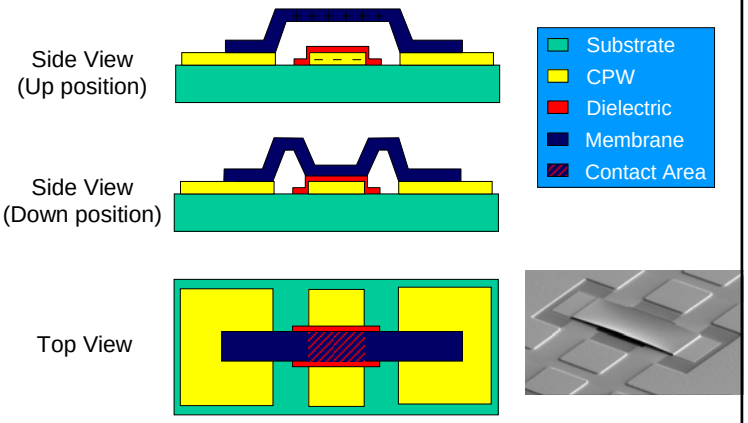
- Fewer processing steps
- Increased feature sizes
- Substrate independent processing
- Lower cost



Surface Micromachining Steps

- Lithography
  - Alignment
  - Resolution
  - Masking
- Material Deposition
  - Material Selection and Properties
  - Conformance
- Sacrificial Etching
  - Stiction

Basic Switch Design



Process Flow

1. Pattern and evaporate 1st metal layer.
   - 200 Å Ti, 3000 Å Au
   - Metal lift-off process
   - 3” GaAs substrates

Questions:

1. What substrate should we use?
2. What material should we use?
3. How do we deposit the first layer?
4. How do we pattern the first layer?

Substrate Choices

- Substrate Requirements:
  - MUST be flat
  - Compatible with all processes
- Desired attributes
  - Cheap and available
  - Easy to work with
  - Device specific
- Material choice
  - Device specific

Problems with Substrate Independence

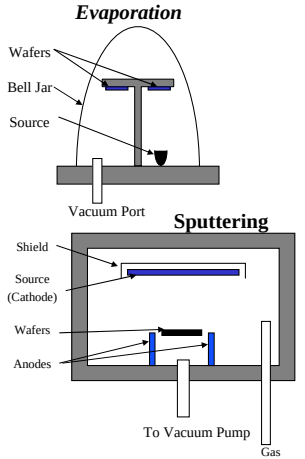
- Surface quality:
  - Roughness
  - Uniformity
- Process and equipment compatibility
  - Adhesion
  - Type of substrate (square or round)
  - Etch steps
  - Photoresist

Example Substrates

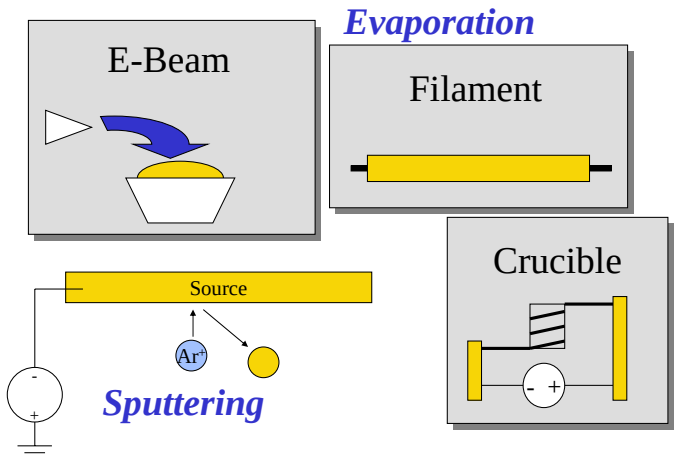
- Silicon
  - Cheapest and Largest area (up to 300 mm diameter)
  - Low resisistance
  - Most widely used
- Gallium Arsenide
  - Fragile
  - Sizes up to 150 mm
  - Most commonly used RF Substrate
- Sapphire
  - Exceptional RF Substrate
  - High ε_r
- Quartz

Fabrication Processes

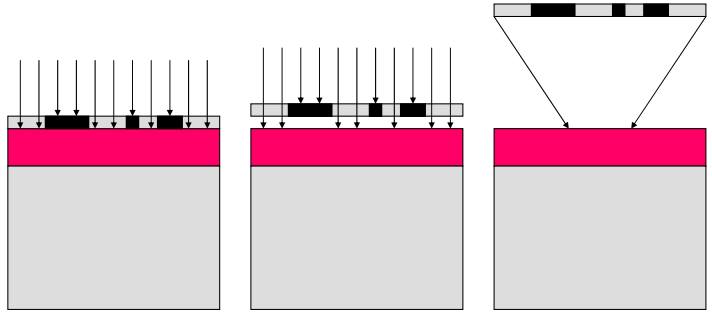
- Primary Metal Deposition Techniques
  - Sputtering
  - Evaporation (E-beam)
  - Electroplating
- Commonly used metals
  - Adhesion layers: Cr and Ti
  - Aluminium
  - Gold
  - Copper
  - Nickel



Evaporation/Sputtering

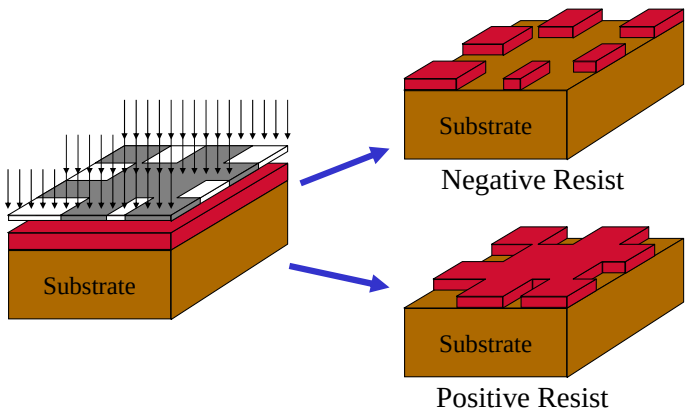


Exposure

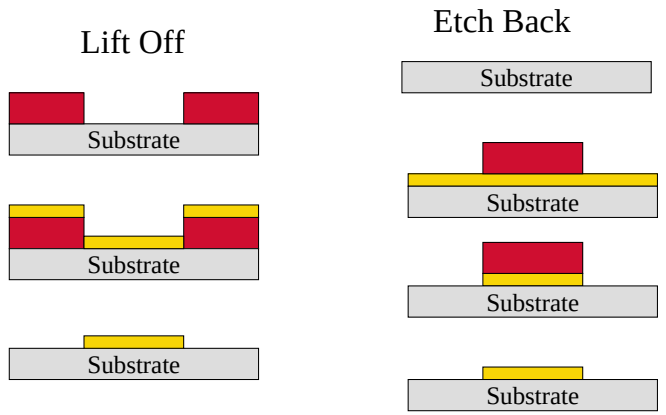


Contact Proximity Stepper: Typically reduces image

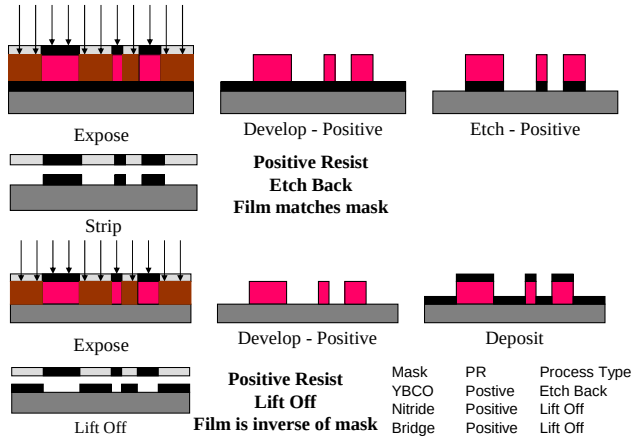
Lithography



Patterning



Exposure



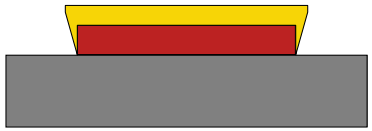
Mask	PR	Process Type	Image
YBCO	Postive	Etch Back	Copy
Nitride	Positive	Lift Off	Inverse
Bridge	Positive	Lift Off	Inverse

Patterning

- Lift off
  - Often results in wings
  - Does not require as many chemicals
  - Limits Process Temperatures
- Etch Back
  - Often provides better results
  - Etch can be done with a variety of techniques
  - May be undercut problems

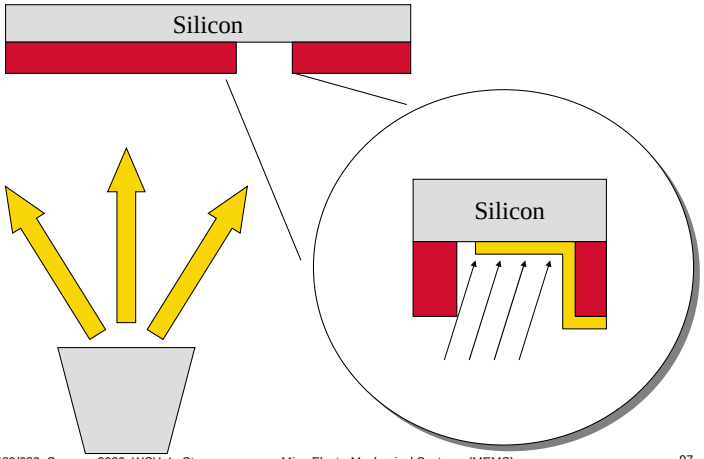
Conformance

The deposition of a material onto a non-planar surface often results in a poor coating of the sides of a structure

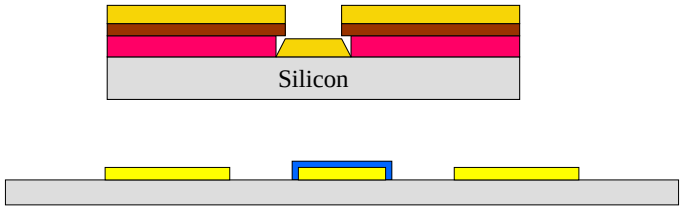


This can result in two layers that were supposed to be isolated being connected

Evaporation



Lift-Off



2. Deposit and pattern dielectric material.
   - 2000 Å sputtered silicon nitride
   - Dry etch process (Freon 14)

Questions:
1. What material should we use?
2. How do we deposit this material?

Material Choices

- Device dependent
  - Quality
    - Uniformity
    - Defects
  - Film Properties
    - Material properties
    - Mechanical properties

Silicon Dioxide (SiO_2)

- Most commonly available
- AKA
  - Phosphosilicate glass
  - Borosilicate glass

SiO_2 Properties

Deposition Method	Step Coverage	Thermal Stability	Density (g/cm^3)	Refractive Index	Stress (MPa)	Dielectric Strength (10^6 V/cm)
PECVD	Varies	Looses H	2.3	1.47	300 C to 300 T	3 to 6
Thermal	Conformal	Excellent	2.2	1.46	300 C	4?

Silicon Nitride (Si_3N_4)

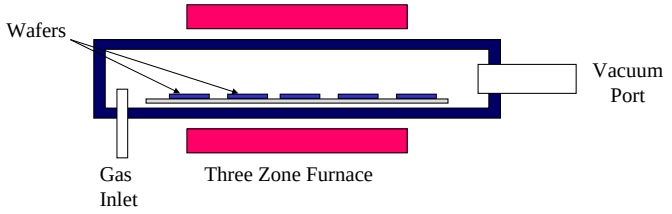
- Excellent Dielectric
- Requires Boiling Phosphoric Acid for a wet etch
- Excellent barrier for Alkali ions

Si_3N_4 Properties

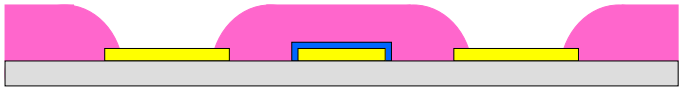
Deposition Method	Deposition Temp. (°C)	Si/N Ratio	Density (g/cm^3)	Refractive Index	Stress (MPa)	Dielectric Strength (10^6 V/cm)
LPCVD	700 - 800	0.75	2.9 to 3.1	2.01	1,00 T	10
PECVD	< 350	0.8 to 1.2	2.4 to 2.8	1.8 to 2.5	200 C to 500 T	5

Fabrication Processes

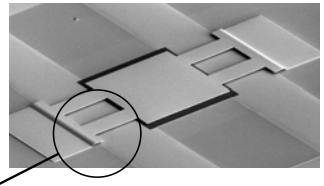
- Common Dielectric Deposition Techniques
  - Sputtering
    - Reactive
  - CVD
    - PECVD
    - LPCVD (Shown)
    - APCVD

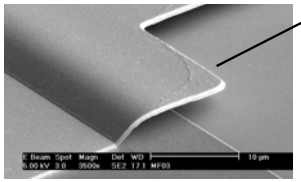


Deposition/Sacrificial



3. Deposit and pattern sacrificial layer.
   - PMGI resist
   - 2 µm - 5 µm thick
   - Reflow above 200 ºC



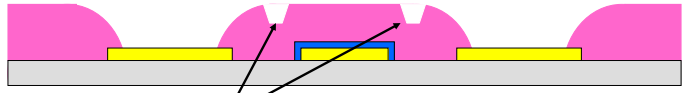


Questions:
1. What material?
2. Patterning?

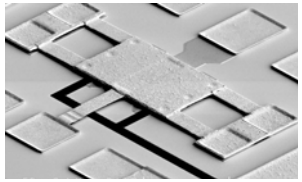
Sacrificial Layer Choices

- Requirements
  - Selective etch available
  - Compatibility
- Materials
  - Polymers (Photosensitive?)
  - Oxides (SiO_2)
  - Metals
  - Others (Silicon)
- Considerations
  - Profile
  - Processing limitations

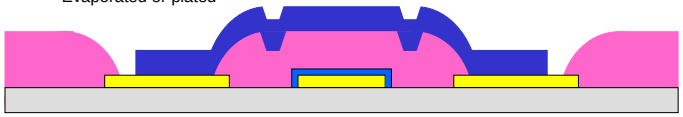
Dimple/Bridge Metal



4. Etch bridge dimples in PMGI
   - Landing bumps
   - Metal-to-metal contacts



5. Pattern and deposit bridge metal.
   - 200 Å Ti, 6000 Å Au
   - Evaporated or plated

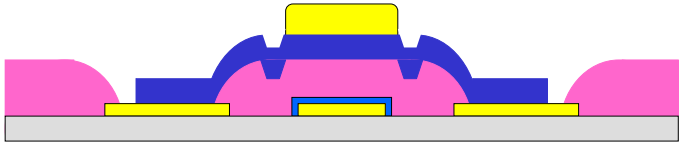


Questions:
1. Why Dimples?
2. How are they formed?
3. Bridge material?

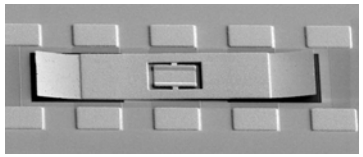
Polysilicon/ Deposition Concerns

- Also Widely Used
  - High value resistors
  - Piezoresistors
  - Mechanical structures
- Typically Deposited with LPCVD
- Doped *in-situ*
- Thin Film Properties
  - Stress
  - Young's modulus
  - Thermal properties (stability, expansion, conductivity)
  - Ion penetration
  - Step Coverage
  - Uniformity/Pinhole defects
- IC Compatibility
- Availability

Bridge Metalization

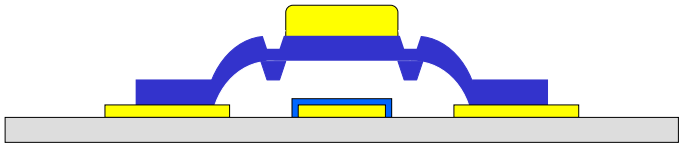


6. Plate overlay layer
   - 3 µm - 5 µm plated gold
   - Strengthen bridge landings
   - Compensate stress gradients

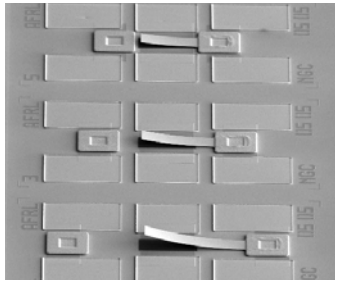


Questions:
1. Material?
2. Deposition?

Release

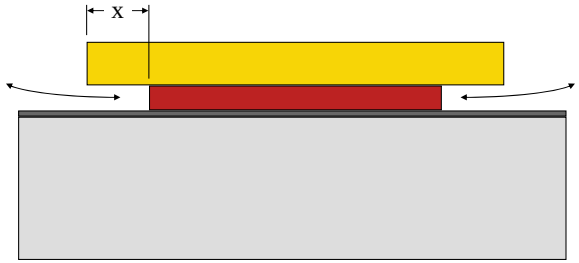


7. Remove PMGI sacrificial layer
   - Wet release process
   - All organic solvents
   - End with acetone
   - Boil off acetone in vacuum



Sacrificial Etch

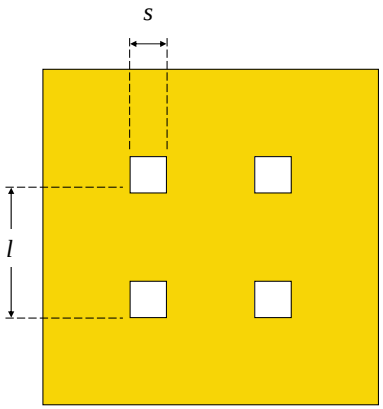
The etch rate (x/t) is diffusion limited



Note that the etch rate may slow down over time

Structural Layer (Au)
Passivation Layer (Nitride)
Sacrificial Layer (Polyimide)
Substrate (Silicon)

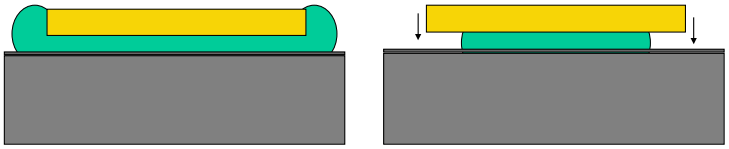
Etch Holes



- Etch Holes are placed with a maximum center to center spacing, *l*
- The etch holes must have a minimum size, *s*

Stiction

- When two flat, smooth surfaces come into contact they tend to stick
- This is a problem
  - During the release process
  - During device operation
- During the drying process, the water evaporates slowly from under the released structures



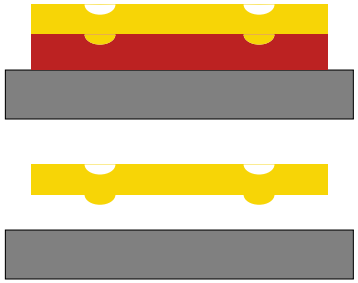
- The evaporation of the water results in an attractive force pulling the released structure towards the substrate
- When the surfaces come into contact they are held together by atomic bonds

Stiction

- This problem can be solved by several methods
  - Coating the structures with a solution
  - Optimizing the temperature
  - Final Methyl Rinse
  - Dimples

Stiction (Dimples)

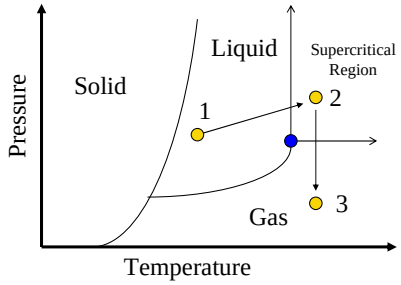
- Dimples are formed by partially etching the underlying sacrificial layer
- The deposited structural layer is then contoured around the indentation
- Dimples prevent large flat areas of the substrate from coming into contact, thus reducing the effect of stiction



Stiction (Critical Point Dryer)

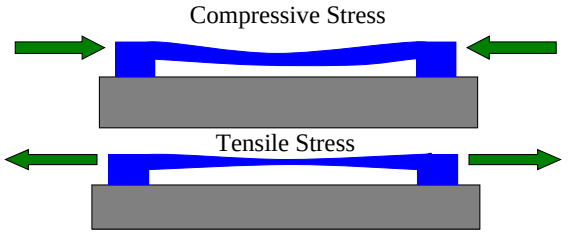
- Use Supercritical Region where there is no surface tension, and liquid and gas phase are blurred

For CO_2, the Supercritical point is 31.1 °C and 72.8 atm (1073 psi)



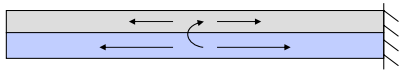
Thin Film Properties

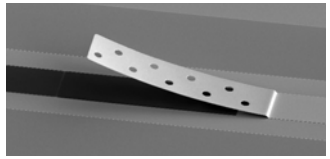
- Not well understood
  - Properties are often not uniform
  - Variation from run to run
  - Polycrystalline materials
- Material Stresses
  - Buckling
  - Change in Mechanical Properties



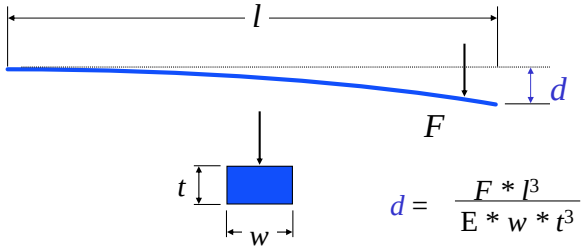
Thin Film Properties

- Stress gradients:





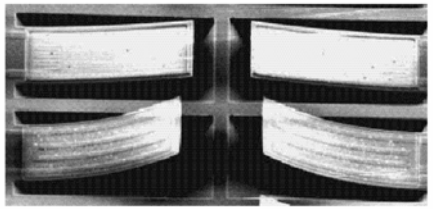
- Young's Modulus Varies

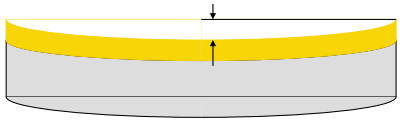


$$d = \frac{F * l^3}{E * w * t^3}$$

Measuring Stress

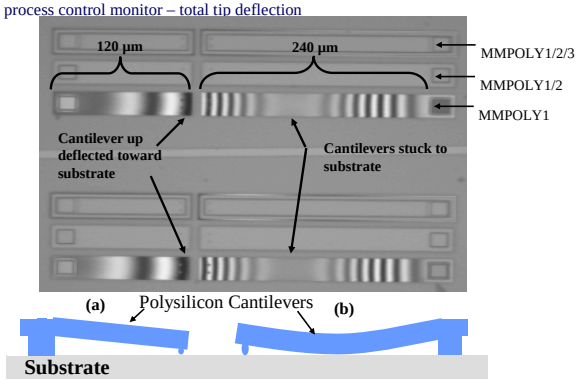
- Wafer Bow
  - Not Accurate locally, or for actual release values
- MicroRaman
  - Allows local stress measurement
  - Non-destructive
  - Pre-release
- Test Structures
  - Cantilevers
  - Buckled Beams
  - Guckel Rings
  - Pointers





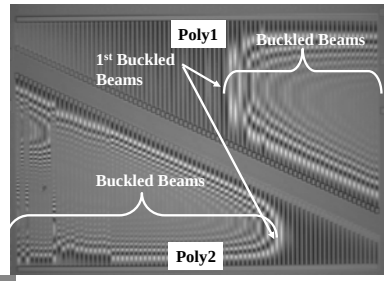
Cantilevers

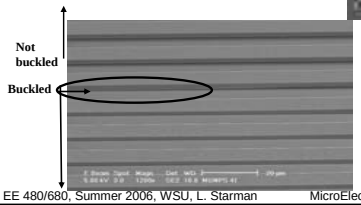
- Cantilevers
  - Measured with an interferometer
  - Gives a 'feel' for stress effects, but is not accurate
  - Provides a process control monitor – total tip deflection



Buckled Beams

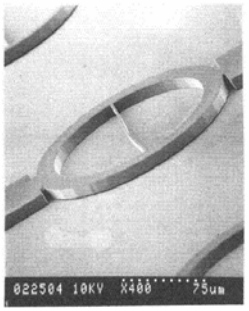
- Buckled Beams
  - Arrays can be used to get a good estimate of compressive stresses
  - As a PCM, they take up a lot of space
  - Visually readable

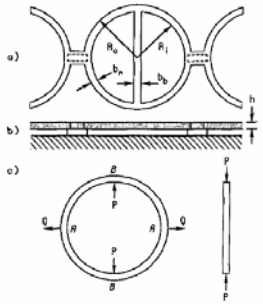




Guckel Rings

- Guckel Rings
  - Allows measurement of tensile stresses
  - Must have a good knowledge of the stress to be effectively used

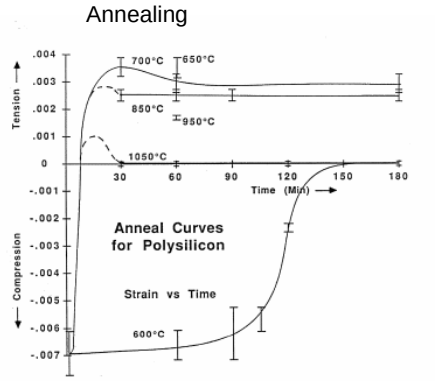




Images from "Diagnostic microstructures for the measurement of intrinsic strain in thin films," H. Guckel, *et al*, J. Micromech. Microeng. 2 (1992) 86-95.

Controlling Stress

- Design
- Multiple layers
- Thicker materials
- Deposition
  - Substrate heating
  - Process parameters
- Annealing
- Ion Implantation

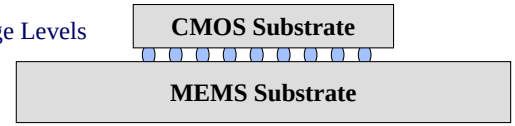


Graph from University of Wisconsin -Work done by Prof. H. Guckel http://mems.engr.wisc.edu/research/strain

IC Compatibility

- Material Selectivity
  - Sacrificial Layer
- Temperature
  - Annealing
- Current and Voltage Levels
- Solutions
  - Packaging
  - Modify MEMS Processes
  - Isolation

Flip Chip Technology

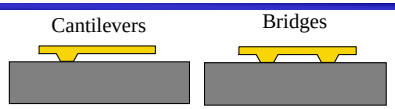


Building Blocks

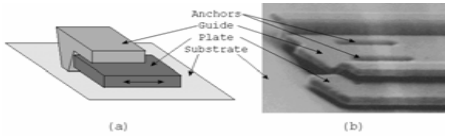
Single Layer Structures
2 Poly

Cantilevers

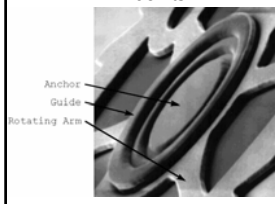
Bridges



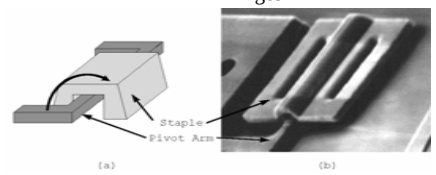
Two Layer Structures/3 Poly
Sliders



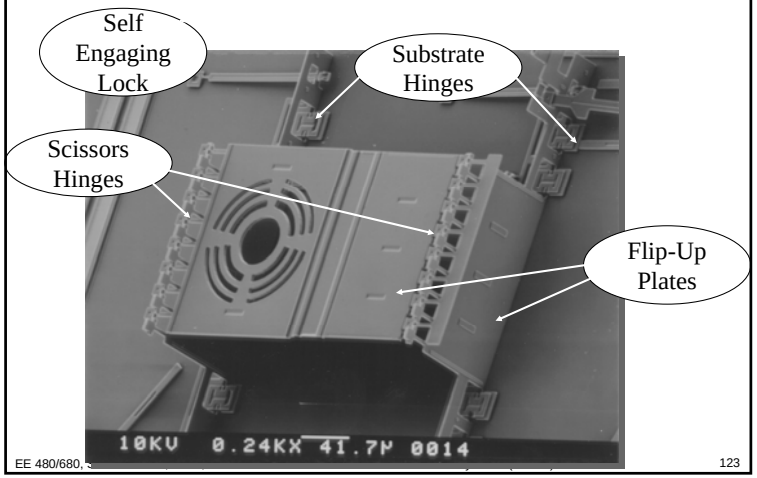
Two Layer Structures/3 Poly
Pin-Joints



Two Layer Structures/3 Poly
Hinges

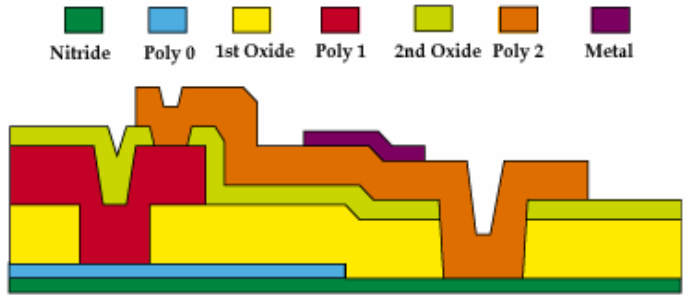


Building Blocks –Flip-Up Structures



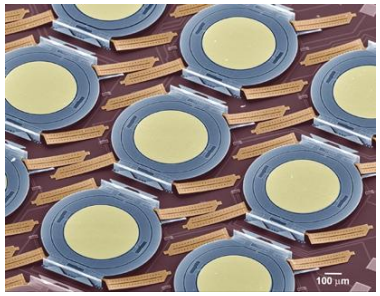
Surface Micromachining

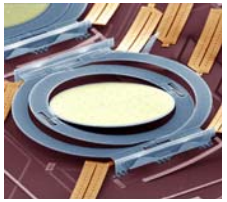
DARPA Sponsored Multi-User MEMS Process (MUMPs)

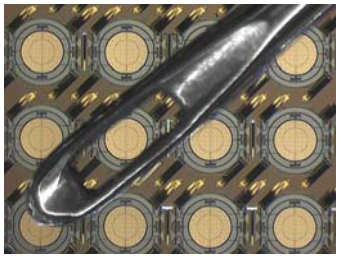


mems.mcnc.org/mumps.html

Lucent LamdaRouter mirror

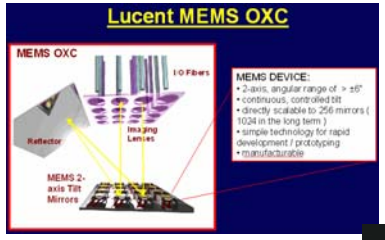


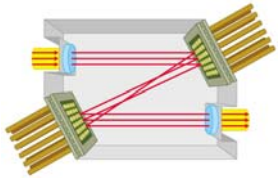


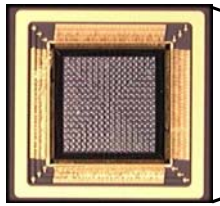


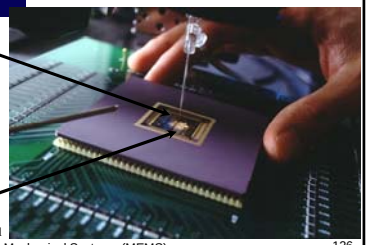
Picture from http://www.bell-labs.com/news/1999/november/10/single_color.tiff

Lucent LamdaRouter Operation



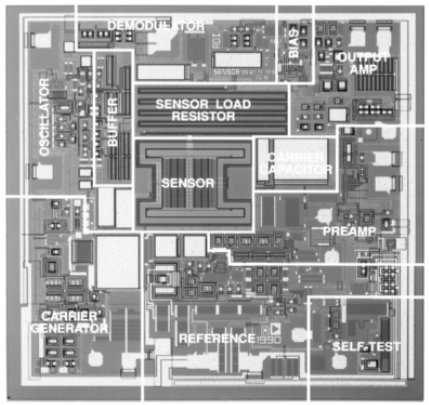






http://www.bell-labs.com/org/physicalsciences/projects/mems/mems3.html

iMEMS



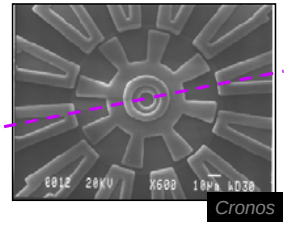
Analog Devices' ADXL-50, the industry's first surface micromachined accelerometer, includes signal conditioning on chip.

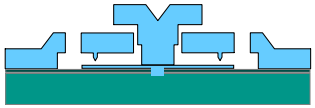
Comparing iMEMS and MUMPS

Process	iMEMS	poly MUMPS
Masks	27	8
Processing Steps	> 410	>70
Structural Layers	1	2
Structural Layer Types	Polysilicon	Polysilicon
Layer Thickness	2 - 4	1.5 - 2
Min Feature Size	1	2
Mechanical	Yes	Yes
Integrated Cicruits	Yes	No

Surface Micromachining: Polysilicon

- Ex. The making of an electrostatic micromotor:



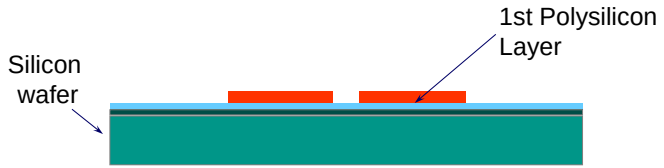


Cross section of motor

Surface Micromachining: Polysilicon

- The first step is to deposit and pattern a layer of structural polysilicon. This layer often serves as a structural base or an electrical path.

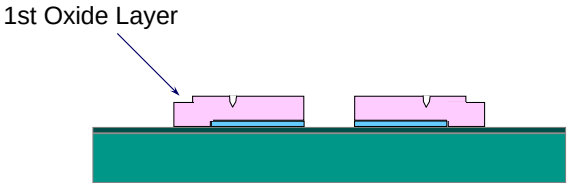
Step 1



Surface Micromachining: Polysilicon

- The second step is to deposit and pattern an oxide sacrificial layer. This layer is used to separate and define the shape of subsequent polysilicon layers.

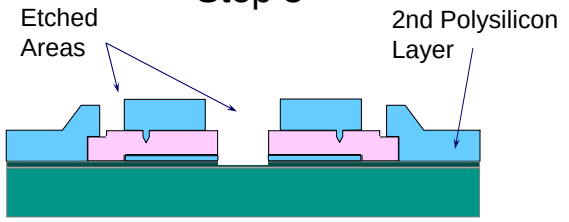
Step 2



Surface Micromachining: Polysilicon

- Next, a second polysilicon structural layer is added and etched to obtain a desired shape.

Step 3

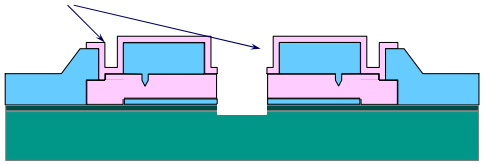


Surface Micromachining: Polysilicon

- Another oxide sacrificial layer is then added and patterned.

Step 4

2nd Oxide Layer

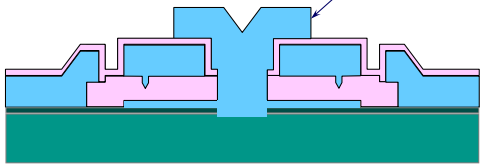


Surface Micromachining: Polysilicon

- The 3rd and final polysilicon structural layer is then deposited and etched to a desired shape.

Step 5

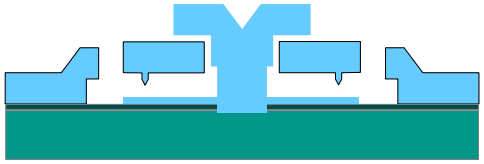
3rd Polysilicon Layer



Surface Micromachining: Polysilicon

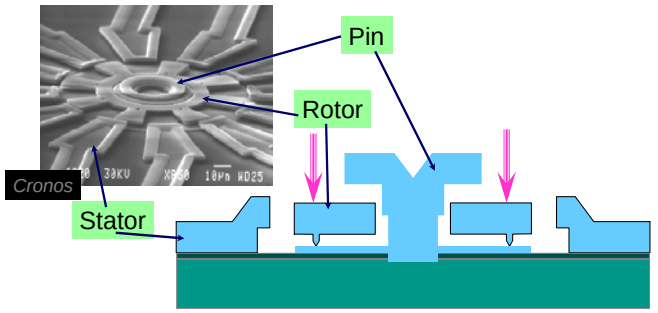
- The final step is to dissolve the oxide sacrificial layers with Hydrofluoric (HF) acid. This leaves behind the complete and free polysilicon MEMS structure.

Step 6: Release



Surface Micromachining: Polysilicon

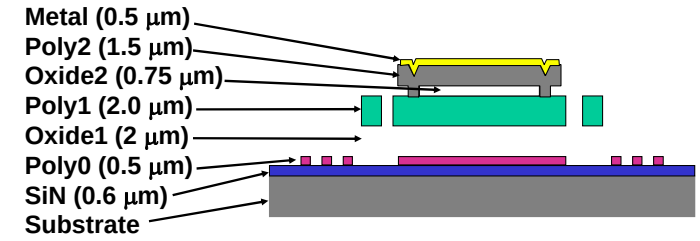
- After the release, all unattached parts usually settle into contact with whatever is beneath them.



MUMPs Fabrication Image

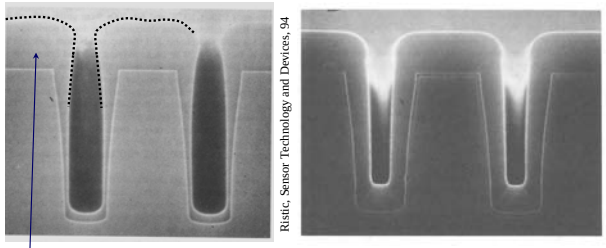
MUMPs Foundry Fabrication
- Primary foundry fabrication used in this research
- Known to exhibit inherent residual stress
- Fairly inexpensive (~ $3,100)
- Timely (new die every 2-months)

MUMPs



Surface Micromachining: Step Coverage

- Conformal or Nonconformal



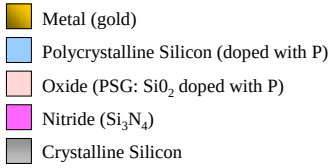
Ristic, Sensor Technology and Devices, 94

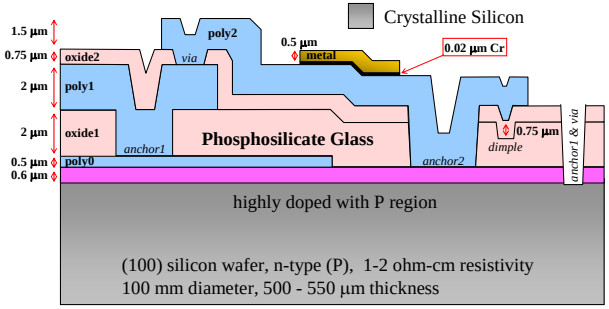
2 μm thick PSG using LPCVD: SiH_4, O_2, and PH_3 at 425 °C and 280 mtorr

2 μm thick PSG using PCVD: TEOS, TMP, and O_2

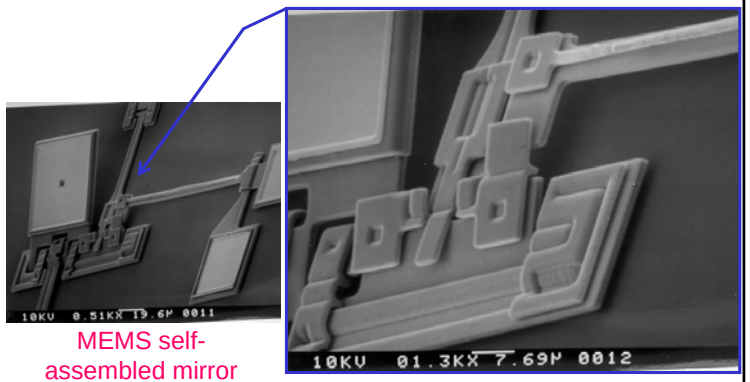
Commercial Surface Micromachining: Polysilicon

- MEMSCAP -- The Polysilicon Multi-User MEMS Processes, or polyMUMPs®
  - Started in 1992
  - www.memscap.com/memsrus/
  - 15 copies of a 1 cm × 1 cm die, $3,200.00





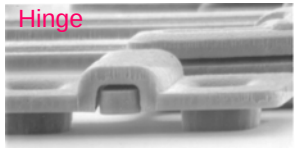
Surface Micromachining: MUMPs Examples



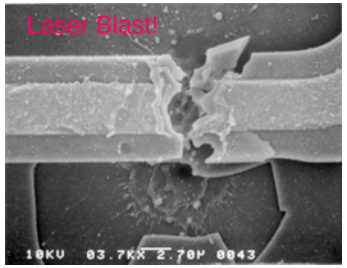
MEMS self-assembled mirror

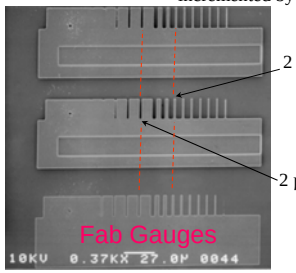
Designed and imaged by J. R. Reid, AFIT

Surface Micromachining: MUMPs Examples



Spaces and widths are incremented by 0.25 μm

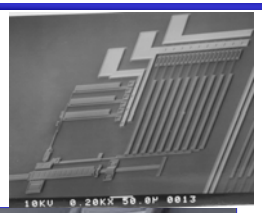


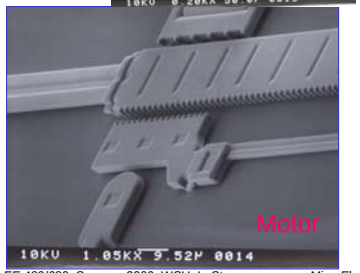


Designed and imaged by P. E. Kladitis, AFIT

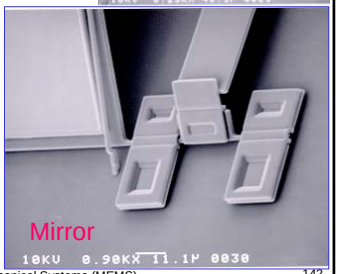
Surface Micromachining: MUMPs Examples

Designed and imaged by J. R. Reid, AFIT

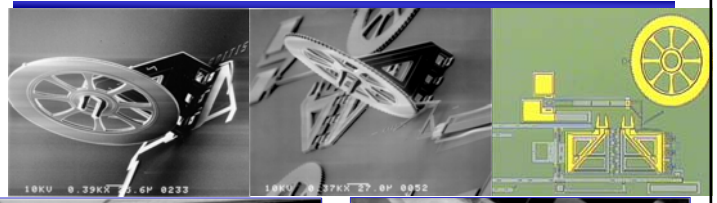




Designed and imaged by W. D. Cowan, AFIT



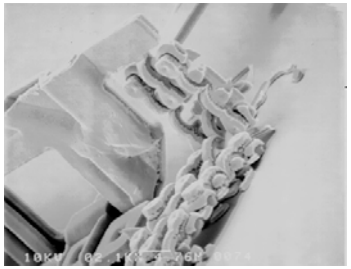
Surface Micromachining: MUMPs Examples



Designed and imaged by P. E. Kladitis

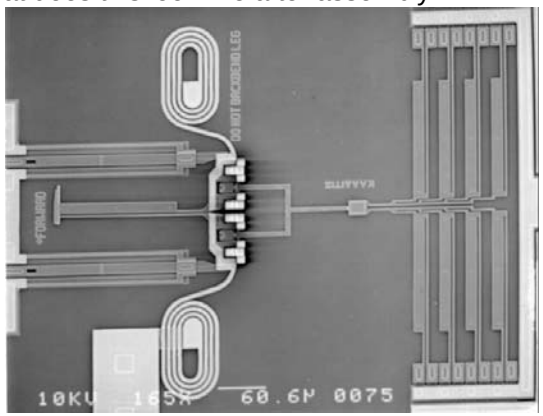
Surface Micromachining: MUMPs Examples

Designed and imaged by P. E. Kladitis

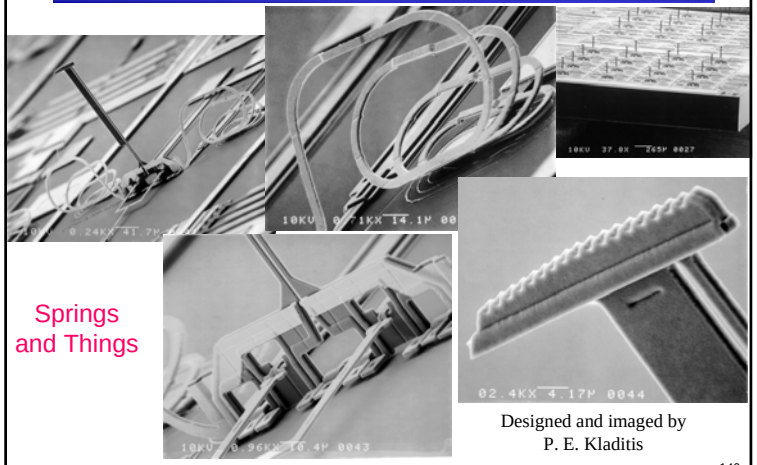


Surface Micromachining: MUMPs Examples

- What does this look like after assembly?



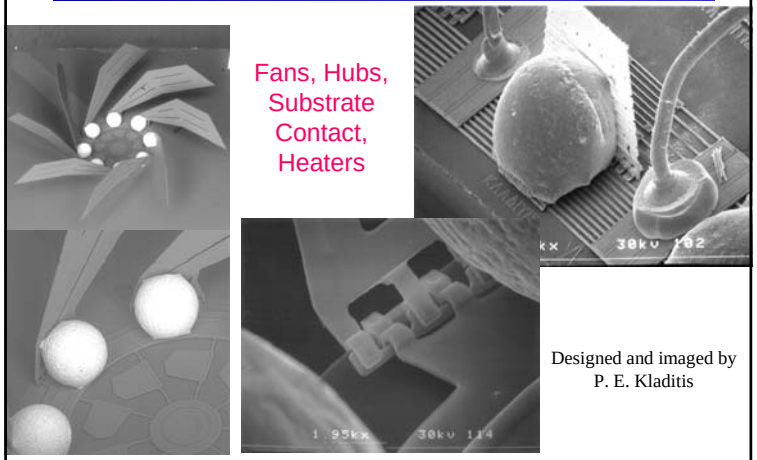
Surface Micromachining: MUMPs Examples



Springs and Things

Designed and imaged by P. E. Kladitis

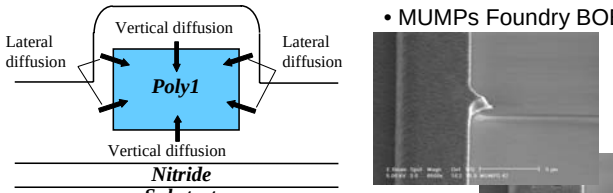
Surface Micromachining: MUMPs Examples



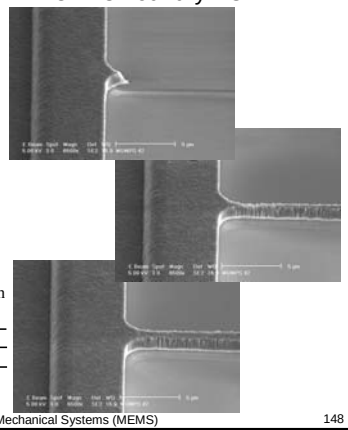
Fans, Hubs, Substrate Contact, Heaters

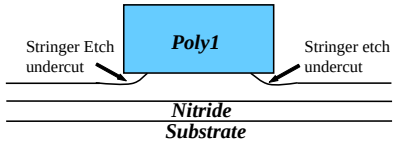
Designed and imaged by P. E. Kladitis

Foundry Fabrication Etch

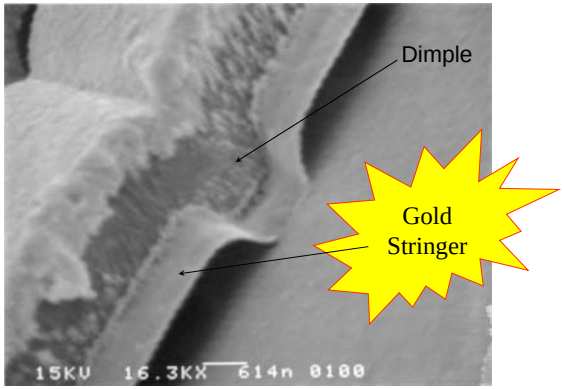


- MUMPs Foundry BOE



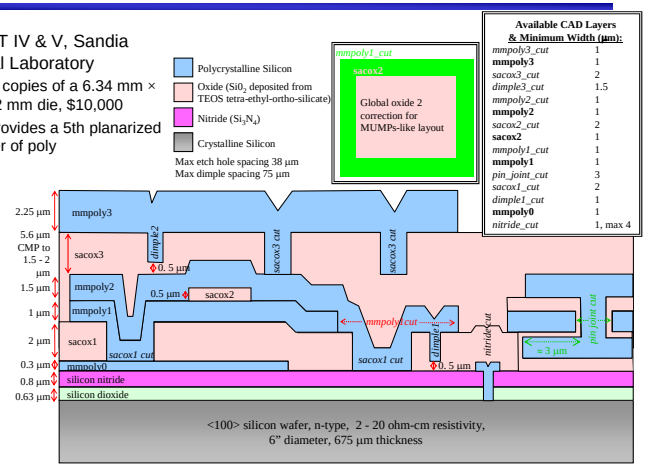


Bonus Slide

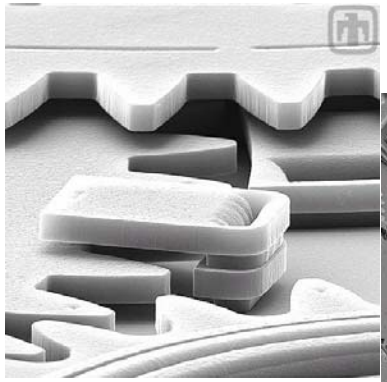


Commerical Surface Micromachining: Polysilicon

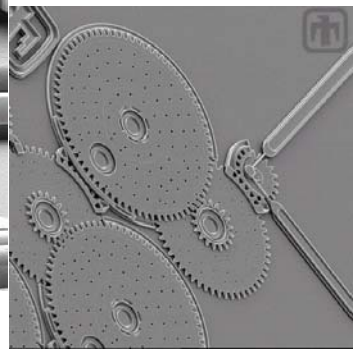
- SUMMiT IV & V, Sandia National Laboratory
  - 100 copies of a 6.34 mm × 2.82 mm die, $10,000
  - V provides a 5th planarized layer of poly



Surface Micromachining: SUMMiT Examples

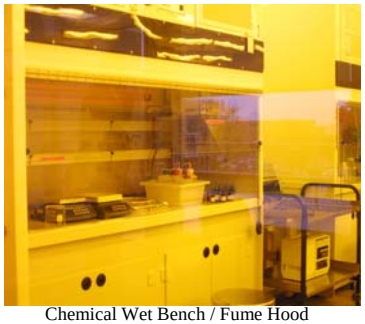


mems.sandia.gov



Surface Micromachining: Release

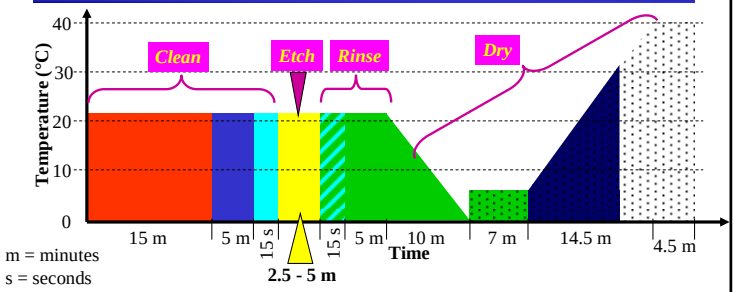
- Wet HF etch removes the P-doped SiO_2 or phosphosilicate glass (PSG)



Chemical Wet Bench / Fume Hood

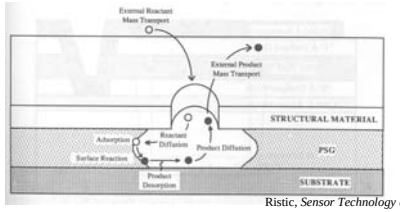
Critical Point CO_2 Dryer
31 °C and 7.38 MPa

Surface Micromachining: Release



Surface Micromachining: Release

- Release Failure Mechanisms
  - Insufficient etch times, temperature, PSG phosphorous content
  - Insufficient number of etch holes
    - for 2.5 - 5 minute etch times, etch holes should be 30 µm apart for MUMPs type designs
  - Allowing surface tension forces, of drying rinse fluids, to pull microstructures against the substrate causing permanent adhesion …. this phenomena is sometimes called stiction

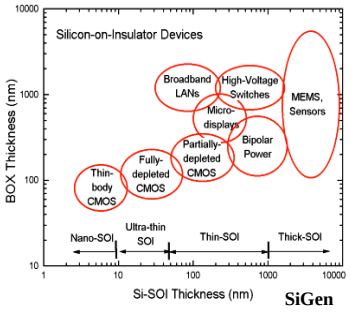


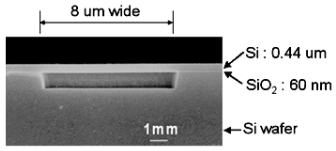
Ristic, *Sensor Technology and Devices*, 94

Silicon On Insulator (SOI)

- Si Bulk Micromachining
  - The creation of microstructures by bulk etching of material from the substrate by (an-)/isotropic wet/dry etching or reactive ion etching.
- Surface Micromachining
  - The creation of microstructures by the selective patterning of thin films and a sacrificial etch.
- SOI
  - Combining bulk etching and a sacrificial etch gives Silicon On Insulator (SOI).
  - Anodic or Fusion Bonded, commercially produced or made in-house.

Silicon On Insulator (SOI)

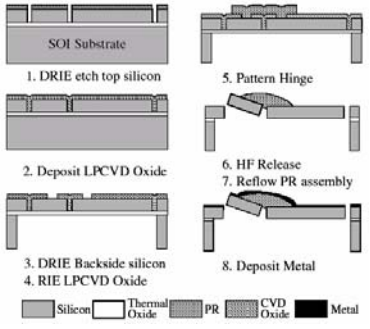


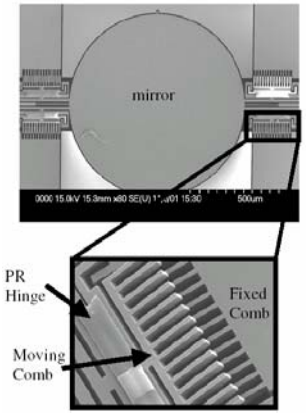


C. H. Yun and N. W. Cheung
Electronics Research Laboratory
University of California, Berkeley
yunch@EECS.Berkeley.EDU
IEEE SOI-98

Silicon On Insulator (SOI): Example

- A scanning micromirror with angular comb drive actuation -- P. R. Patterson, et al., 2002.



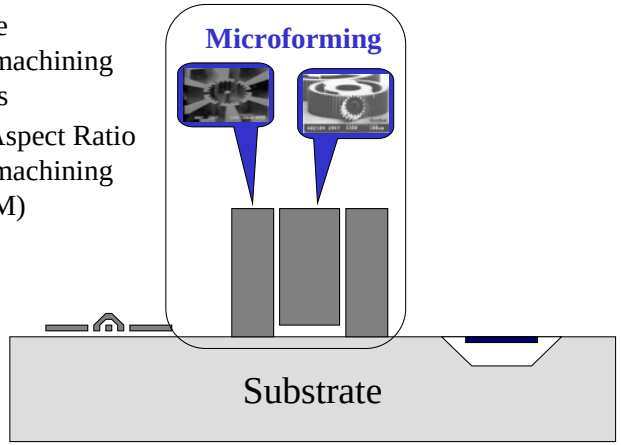


Overview

- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

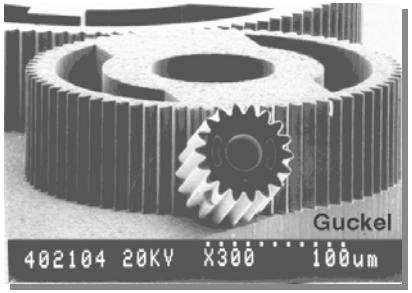
MEMS Fabrication

- Surface Micromachining Process
- High Aspect Ratio Micromachining (HARM)



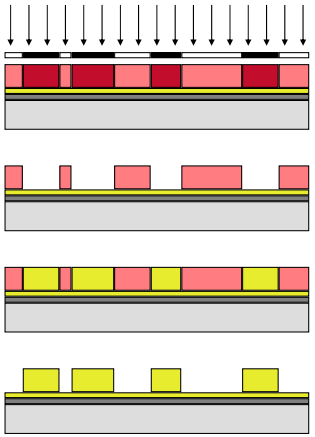
Microforming

- Grow what you need
- Basic process is generally simple
- High Aspect Ratio Structures
- MEMS Specific
- Typically Metal
- Aspect Ratio



SEM from mems.mcnc.org

Microforming

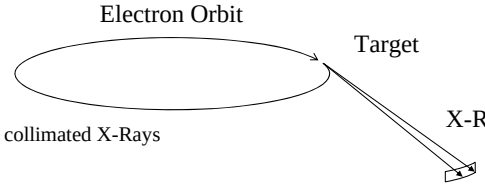


LIGA

In German:
Lithographie, Galvanoformung, Abformung

- Requires Highly Collimated X-Ray source such as an X-Ray Synchrotron
- Resist is Polymethylmethacrylate (PMMA)
- Aspect Ratios over 100!
  - Comparable with Anisotropic Wet Etching

Synchrotron Radiation



- Provides
  - High intensity collimated X-Rays
- But
  - Requires expensive facilities (>$ 30 M)

LIGA

Masking

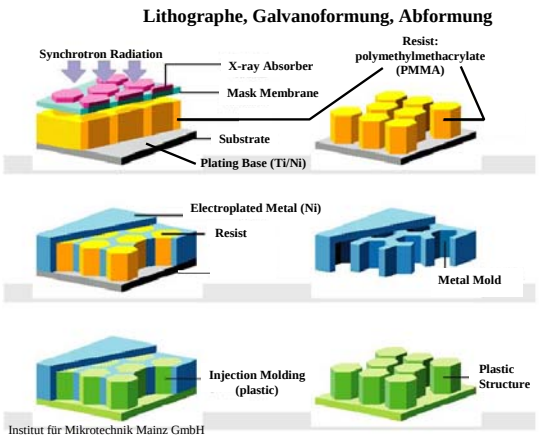
> 10 μm thick

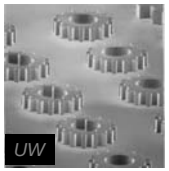
- Requires special masks
  - Cost per mask can exceed $10,000

Deposition

- Electroplating
- Electroless plating
- Primary difficulties
  - Thickness (over 100 μm)
  - Stress
- Selective CVD

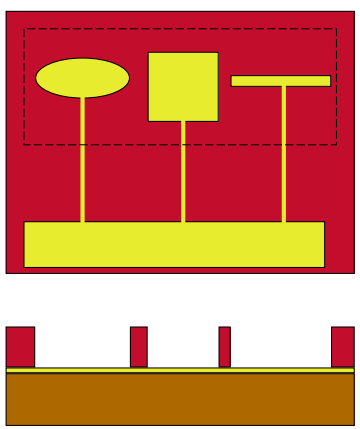
Micromolding: LIGA

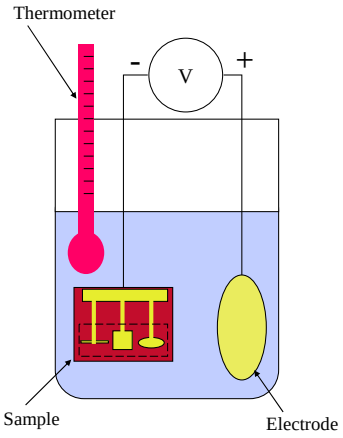




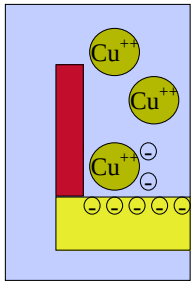
SLIGA: when the plating base or other material is used as a sacrificial layer under the metal.

Electroplating





Electroplating



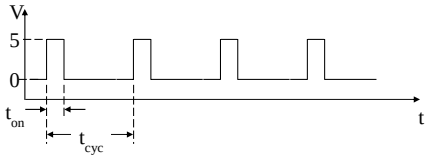
$Cu^{++} + 2e^- \Rightarrow Cu(s)$

$Au(CN)_2^- + 2e^- \Leftrightarrow AuCN + CN^-$

$AuCN + e^- \Leftrightarrow Au(s) + CN^-$

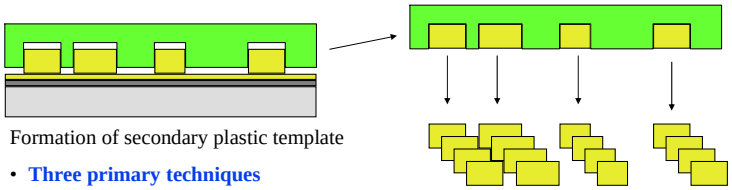
Pulsed Electroplating

- Typical pulse parameters
  - 1 kHz
  - 10% Duty Cycle
- Provides
  - Better stress control
  - More uniform Deposition



Molding

The cost of the X-Ray exposure, and mask are offset by using the metal parts not as an end product, but instead as a mold.

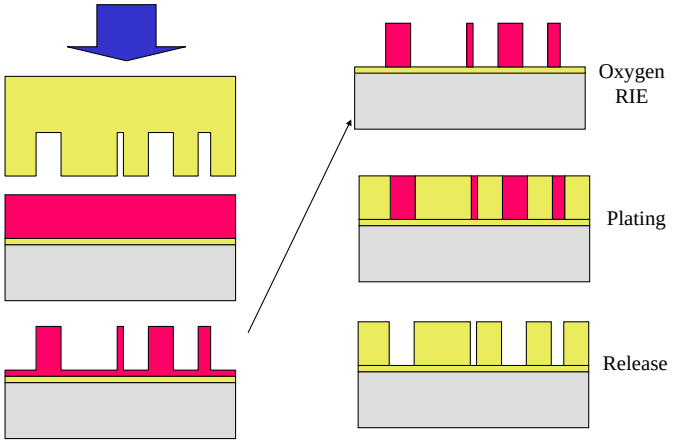


Formation of secondary plastic template

Electroplating to form metal parts

- **Three primary techniques**
  - Reaction Injection Molding
    - Mix polymers just before injection
  - Thermoplastic Injection Molding
    - Heat the polymer to a viscous state
  - Impression molding
    - Printing Process
    - Primary technique used in German processes

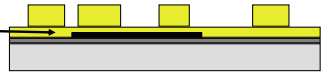
Impression Molding



Sacrificial Processes

A sacrificial layer can be added to the process

Sacrificial Layer

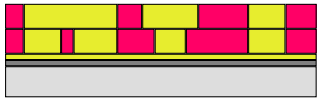


After the PMMA is removed, the seed layer and the sacrificial layer are etched away

Multilayer Processing

By planerizing the surface, a second layer can be added.

The process can also be used in conjunction with surface micromachining processes.



LIGA Limitations

- COST!!
  - •X-Ray source availability
  - •Masks
- Typically only one layer
- Radiation Damage

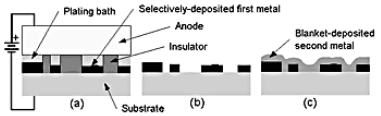
SU-8 – Example Polyimide

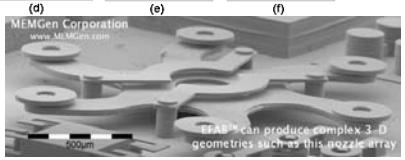
- Developed by IBM
- UV exposer 350-400 nm
- Aspect ratios greater than 20:1
- Thickness over 200 microns
- Primary difficulty
  - •Epoxy based resist that is difficult to strip

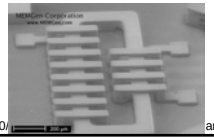
Deep UV Processes

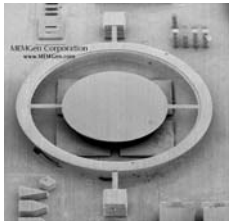
- Poor Man's LIGA
- Replace PMMA and X-Rays with Photosensitive Polyimide and Deep UV (240 nm) exposure
- Aspect Ratios > 10
- Structures up to 30 μm tall
- Availability
- Standard Lab Environment

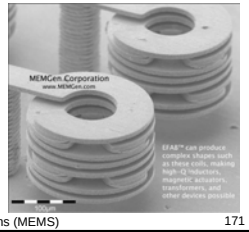
EFAB











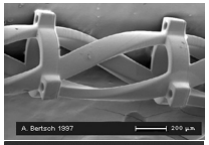
Micromolding: Other

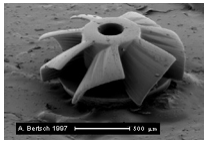
- Laser Machining
  - Heat treatment
  - Welding
  - Ablation
  - Deposition
  - Etching
  - Lithography
  - Photopolymerization
  - Microelectroforming
  - Focused-beam milling of plastics, glasses, ceramics, metals

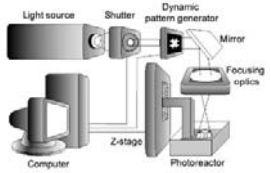
List compiled from M. Madou, *Fundamentals of Microfabrication*, 1997

Micromolding: Other

- Micro-Stereo-Lithography (MSL)
  - Objects are built layer by layer.
  - An image (UV light) of the layer to be built is generated and projected onto the surface of a photopolymerizable resin.
  - A selective polymerization of the liquid resin occurs in the irradiated areas.
  - A shutter cuts out the light when the layer is solidified.
  - The polymerized object is then lowered in the photoreactor, immersing it slightly in fresh resin.
  - When the liquid surface has been stabilized, the irradiation of the next layer can be started.



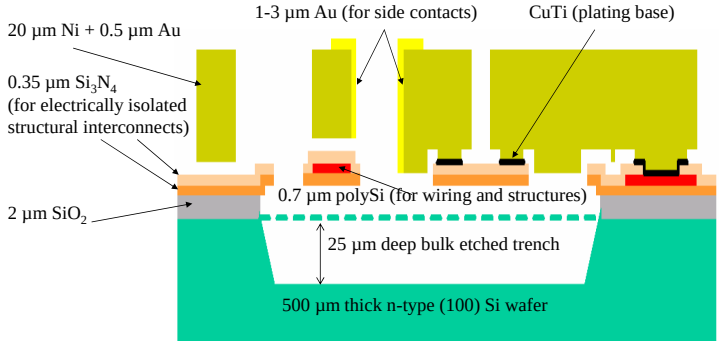




Dept. of Microtechnique, Swiss Federal Institute of Technology, Lausanne

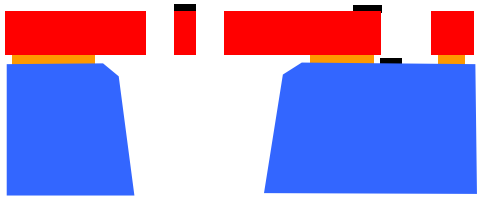
Other Miscellaneous Commercial Micromachining

MetalMUMPs - 10cm wafer fab



Other Miscellaneous Commercial Micromachining

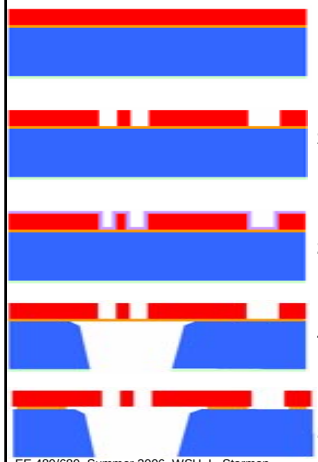
SOIMUMPs



Material Layer	Thickness (µm)	Lithography Level Name	Lithography Level Purpose	Comments
Silicon	25.0	SOI	Define structures in Silicon layer of SOI wafer	
Oxide	2.0			
Substrate	400	TRENCH	Define through-hole structures in Substrate layer of SOI wafer	
Metal	0.7	METAL	Pattern through holes in shadow mask. The shadow mask is then bonded to the SOI wafer so that a patterned Metal layer is achieved when the Metal is deposited.	40nm Ti + 60nmPt + 600nm Au

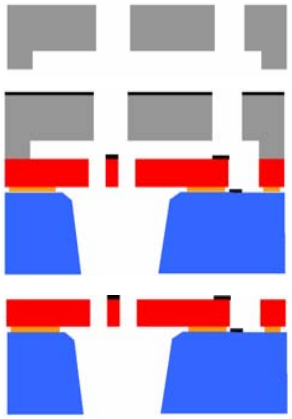
Mnemonic level name	CIF level name	GDS level number	Minimum feature (µm)	Minimum space (µm)	Maximum feature length (µm)	Maximum patterned (etched) area
SOI	SOI	10	2*	2* or 8 (see Section 2.2.1)	N/A	33 mm^2
TRENCH	TRCH	20	100	200	5000	20 mm^2
METAL	METL	30	50	50	5000	20 mm^2

SOI MUMPS



1. Begin with silicon on insulator wafer, 25 µm top silicon layer, 400 micron thick substrate, 2 mm oxide. A back side oxide is also present
2. Lithographically pattern a photoresist on top of the thin silicon layer. Etch down to the oxide using the photoresist as a mask. Strip the resist.
3. Blanket coat the top with a PSG layer. Anneal at 1050°C in argon to dope the silicon. Strip the PSG in a wet etch.
4. Lithographically pattern photoresist on the back side of the wafer. Use DRIE to etch through the wafer, stopping on the oxide. Strip the photoresist
5. Remove the oxide in a buffered oxide etch

SOI MUMPS

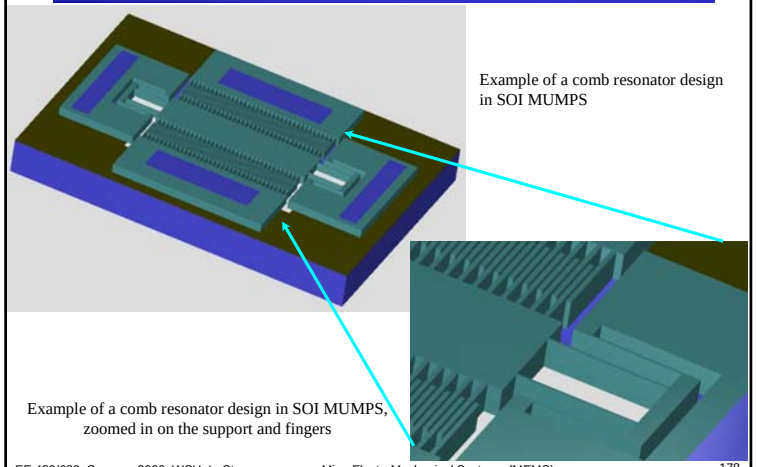


6. A shadow mask is created out of a second silicon wafer.

7. The shadow mask is temporarily bonded to the top silicon layer, and the metal layer is deposited.

8. The shadow mask is removed.

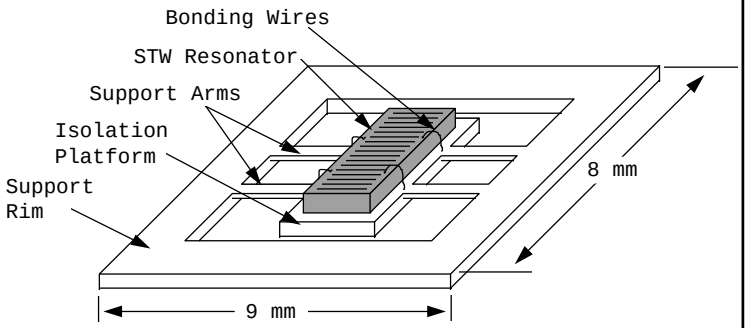
SOI MUMPS



Example of a comb resonator design in SOI MUMPS

Example of a comb resonator design in SOI MUMPS, zoomed in on the support and fingers

Bulk Micromachining



IC Compatibility

- Material Damage
- SiO_2
- Al
- Temperature
- Doping
- Pre- or Post- Processing

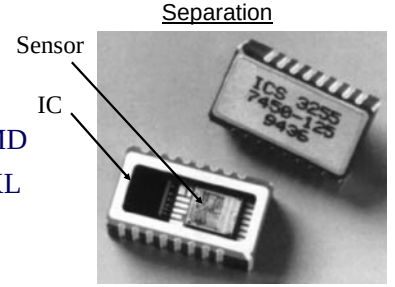
Overview

- Materials
- Microelectronics Fabrication
- Bulk Micromachining
- Surface Micromachining
- Micromolding
- Packaging

IC Compatibility

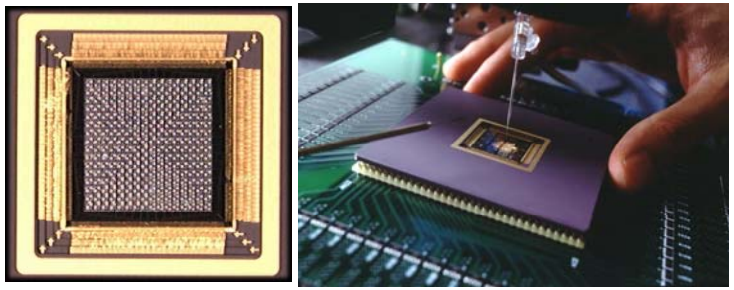
- Separation
  - System in a Package – Ex. IC Sensors
  - Flip Chip
- Integration
  - MEMS First – Ex. DMD
  - Integration – Ex. ADXL
  - IC First – Sandia

Separation



Picture from IC Sensors Application notes: Model 3255 Accelerometer

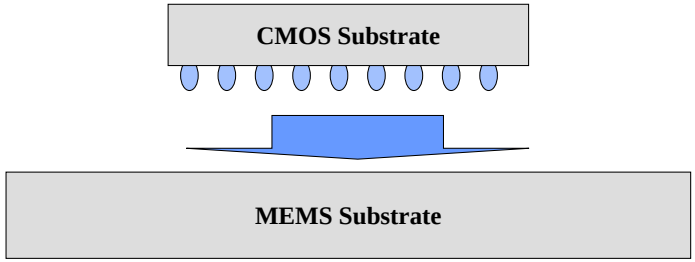
Lucent LamdaRouter Packaged Die



http://www.bell-labs.com/org/physicalsciences/projects/mems/mems3.html

IC Compatibility

Flip Chip Technology



IC Compatibility – IC First

EE M250B

Fabrication of DMD

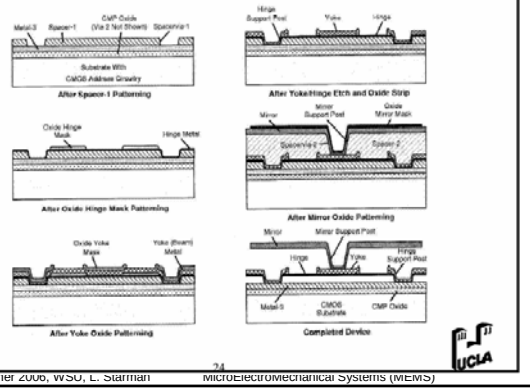
- Use aluminum instead of polysilicon as structural material
  → Completely compatible with CMOS
- Use DUV-hardened photoresist for sacrificial material
  → Dry releasing in Plasma Etcher to reduce stiction
- Aluminum alloys are used to improve performance
  - Al mirror may contains a small fraction of Cu and Si
  - One report mentioned 0.2% Ti, 1% Si is added to Al hinges. Al compounds for anti-creep were discussed.
- DMD superstructure built on CMOS memory (SRAM) circuit
- 6 photomask layers

M. C. Wu 23 UCLA

IC Compatibility – IC First

EE M250B

Fabrication Process Flow



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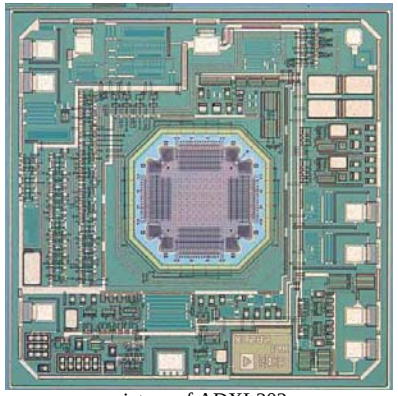
MEMS Fabrication



picture of ADXL202
from www.analog.com

IC Compatibility – MEMS First

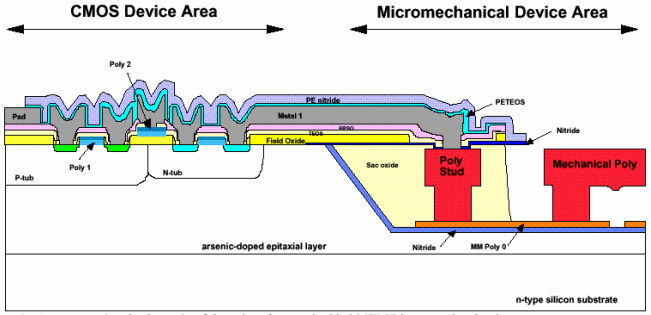


Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

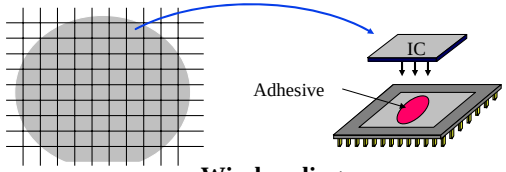
Picture from: J.H. Smith, et al.,"Characterization of the embedded micromechanical device approach to the monolithic integration of MEMS with CMOS," SPIE Micromachining and Microfabrication '96

IC Integration

- **MEMS First**
  - + **IC fab is not compromised**
  - + **Allows high temperature anneals**
  - – **Can result in difficult interconnects**
  - – **Complicates release**
- **IC First**
  - + **IC Fab is not compromised**
  - + **Most expensive processing done first**
  - – **Limits processing temperatures and thus material choices**
- **Integrated Process**
  - + **Fewest number of steps**
  - – **Greatest complexity**

IC Packaging

- Packaging
  - Puts devices into an easily manipulated container
  - Provides the system with the proper environmental interaction
- Cost of Packaging is non-trivial
  - often 70%-80% of total unit cost
- IC Packaging
- MEMS specific Packaging



Wirebonding

IC Packaging

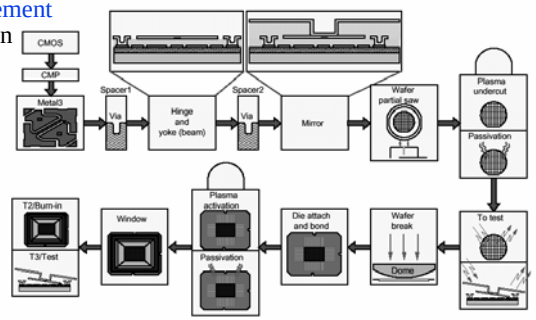
Dicing & Separating → Pick & Place → Wire Bonding → Sealing

- Where do we release
  - What about dust particles
- How do we seal
  - Must maintain free motion
- What about access
  - Optical or pressure interconnects

Primary IC Issues

- Electrical Connectivity
  - Interconnects
  - RF?
- Reliability
  - Au/Al
- Thermal Management
  - Heat Sink/Fan
- Environment
- COST!!!
- Automation

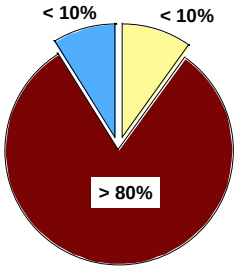
DMD Packaging



Switch Packaging Approaches
(Known Efforts)

Conventional (Chip-in-box) (<10%)
Dice ⇒ release ⇒ package or
Dice ⇒ package ⇒ release
Ceramic / Metal package

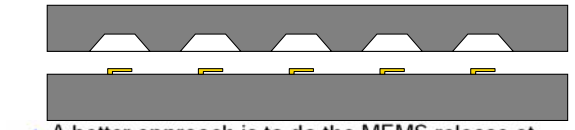
Thin-film Encapsulation (<10%)
Thin-film bubble, cap ⇒
Release through holes ⇒
Seal ⇒ Dice



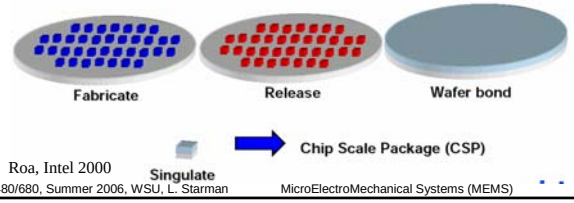
Approaches

Wafer Bonding (> 80%)
Release ⇒
Bond cap wafer ⇒ Dice
Metal eutectic or Glass frit seal

Wafer Level Packaging



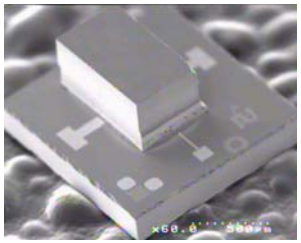
- A better approach is to do the MEMS release at the wafer level.
- Wafer level packaging (WLP) must follow the wafer level release, to avoid damaging the MEMS.
- Much smaller packages are possible

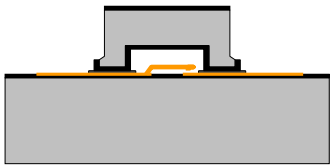


Roa, Intel 2000

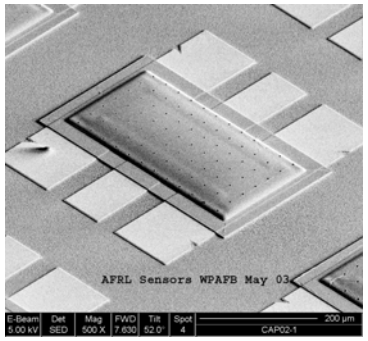
Wafer-Level Cap

- Wafer-to-Wafer Bonding is Employed to Cap the Individual Switch Die
  - Provides Hermetic Environment
  - Low-Cost Packaging Solution
  - Optimization is in Process
- RMI has Produced Fully Functional Devices with Promising RF Results
  - High-Lifetime: >10^{11} Cycles
    - Best Case
  - Optimization of RF Performance is in Process

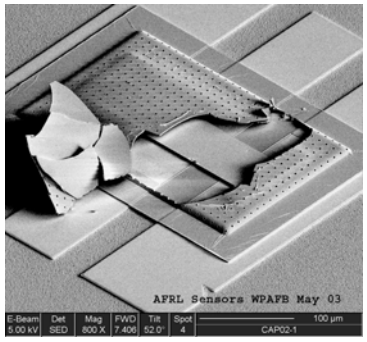




Silicon Nitride Encapsulated Switches



Released switch under nitride cap

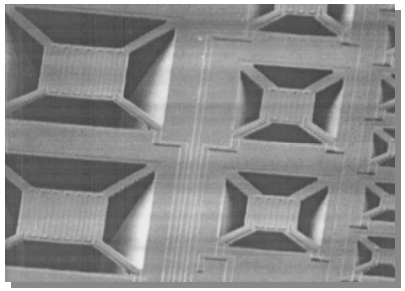


Nitride cap partially removed showing released switch

Fabrication Review

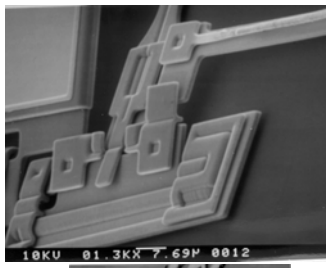
Bulk Micromachining Summary

- Fabrication using bulk material
  - Silicon
- Primary Processes
  - Masking
  - Etching
  - Wafer Bonding
- Large Structures
- Less control over Dimensions
- One to two regions
- Bulk Micromachined Devices
  - Thermal Isolation
  - Reduction of Parasitic in Microwave Devices
  - Seismic Masses
- Primarily Custom Processing



Surface Micromachining Summary

- Fabrication using thin films
  - IC fabrication
- Primary Processes
  - Sacrificial Layer Processes
- Planar well defined processes
- Multiple releasable layers
- Two and half dimensional
- Surface Micromachined Devices
  - Single layer structures
    - Cantilevers
    - Bridges
  - Micro-Hinges and flip up structures
- Primarily Standard IC Processes



Microforming Summary

- Fabrication using deposited films and molding
- Primary Processes
  - LIGA
  - Thick Resist
- High Aspect Ratio Micromachining (HARM)
- Typically 1 layer
- Medium to good resolution

Process Comparison

	Surface Micromachining	Bulk Micromachining	Microforming
x,y dim.	< 1 μm	> 5 μm	> 2 μm
z dim	< 5 μm	> 20 μm	> 20 μm
# Layers	2-3 Releasable	1-2	1 Releasable
IC Compatibility	Good	Med-Poor	Good
Material Selection	Large	Bulk Materials	Metals
Aspect Ratio	< 5	approx. 100	approx. 100

Process Comparison

Process	iMEMS	poly MUMPS	metal MUMPS	SOI MUMPS
Masks	27	8	6	4
Processing Steps	> 410	>70	> 50	>35
Structural Layers	1	2	2	1
Structural Layer Types	Polysilicon	Polysilicon	Nickel, Poly Nitride Poly-Stack	Bulk Silicon
Layer Thickness	2 - 4	1.5 - 2	20,2	25
Min Feature Size	1	2	8	2
Mechanical	Yes	Yes	Yes	Yes
Integrated Cicruits	Yes	No	No	No
Available Die Size	N/A	1 cm X 1 cm	1 cm X 1 cm	1 cm X 1 cm
Cost per die site	N/A	$ 4,600.00	N/A	$ 7,500.00