

**EE/CEG 454(654)**  
**VLSI Systems\***

**INSTRUCTOR:** Dr. John M. Emmert

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**OFFICE HOURS:** W 2:30 pm – 4:00 pm or by appointment

**TEXT:** Weste and Harris, *CMOS VLSI Design, A Circuits and Systems Perspective*, Addison Wesley, 3<sup>rd</sup> Edition, `05

**REFERENCE:**

Hodges, *Analysis and Design of Digital Integrated Circuits*, McGraw Hill, `04  
Kang, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw Hill, `03  
Wolf, *Modern VLSI Design*, Prentice Hall, 3<sup>rd</sup> Edition, `02  
Uyemura, *Introduction to VLSI Circuits and Systems*, Wiley, `02

**TIME:** TR 10:25 pm – 11:40 pm

**PREREQUISITES:**

Courses:

- EE 451(651) or CEG 360(560) Digital Systems Design

Topical:

- Be able to perform digital logic circuit analysis and design
- Understand sequential logic and computer design fundamentals

**LOCATION:** 145 Russ

**DESCRIPTION:** This course covers introductory topics in Very Large Scale Integrated (VLSI) circuit design. We develop several transistor models at various levels of abstraction for CMOS devices and CMOS circuit components. We briefly describe basic steps in the chip fabrication process, but the **main emphasis of the course** is design; we cover several different CMOS design paradigms for Application Specific Integrated Circuits (ASICs). Additionally, at various times throughout the quarter other topics (like chip planning, circuit layout, circuit simulation, and power dissipation) related to VLSI circuit design are covered.

**OUTCOMES:** The following competencies will be imparted and assessed. Each student should (these will be evaluated during the last exam):

1. understand basic electrical properties of FET circuits and components
2. demonstrate the ability to design VLSI circuits using switching logic
3. know chip layers, fabrication processing steps, and design rules
4. understand layout, timing, and power dissipation issues
5. be able to design, simulate, and validate simple VLSI circuits

\* We will adhere to this syllabus as closely as possible. However, I reserve the right to make changes (in the material covered) as necessary in order to meet time constraints.

## TOPIC OUTLINE:

Topics	Note:
Intro	Introduction/Pre-exam
1.1-1.3	History/MOS Transistors
1.4	CMOS Logic
1.4	Transmission Gate Logic
1.10	Physical Design -> Standard Cells
1.11	Design Verification -> Design Rule Check/Simulation
1.5,8.8	Layout of Standard Cells -> Stick Diagrams
1.4	Flip Flops/Latches Timing Issues/Review
2.1-2.3	MOS Transistors/Ideal IV Characteristics and Gate Cap Model
2.5	DC Transfer Characteristics and Noise Margins
2.6	Switch Level RC Models
3.3	Layout Design Rules / Layers
4.2/4.3	Delay Estimation/Transistor Sizing
4.4	Power Disipation
4.5	Interconnect/Elmore Delay Model
4.8.5	Latchup
4.9	Scaling
6	Combinational Circuit Design
7	Sequential Circuit Design
10	Datapath Subsystems
11	Array Subsystems/Memories

## GRADING:

1. Pre-test, 2<sup>nd</sup> class period (10%)
  2. Test 1 (35%)
  3. Test 2 or Final Exam (35%)
  4. Labs / Projects (20%)
- Each test and project will be graded on a 100-point scale.

This is a design-oriented course. The purpose of the labs and projects are to enforce the concepts presented in class. Therefore it is to the advantage of the student to complete all assignments. Quizzes will be given as necessary. They are a tool used to evaluate student and class progress.

The following grading scale will apply:

- A: 90 -100 pts
- B: 80 - 89 pts
- C: 70 - 79 pts
- D: 60 - 69 pts
- E: 0 - 59 pts

## MAKE-UPS:

Make-up exams will only be given for excused absences (*excused in advance*).

## ATTENDANCE:

Students are responsible for all **business** and **material** covered during each and every class.

## CHEATING:

My goal is to treat all students as fairly as possible. Everyone will have an equal opportunity to excel. Cheating will not be tolerated! Anyone caught cheating will be dealt with according to applicable university policy.

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