

CEG 750: Microprocessor
Winter 2011, 4:10 – 5:25 Tue. Thur. at 339 RC

1. **Instructor:** Jack S.N. JEAN

Office Hours: 1-2:10 & 3:40-4:10 PM, Tue., Thr.; 334 RC, 775-5106, jack.jean@wright.edu

2. **Course Format:** The course is project-oriented. The scheduled class time is for project preparation/discussion/group meeting.

3. **References:**

- **The HCS12/9S12: AN INTRODUCTION**, Han-Way Huang, 2nd edition, Delmar Cengage Learning, 2009.
- **Embedded Systems: Design and Applications with the 68HC12 and HCS12**, Steven Barrett and Daniel Pack, 1st edition, Pearson, 2005.

4. **Course Project:**

Design and implement an MC6812 computer system based on an Axiom CSM-12C32 board that allows the loading of a 6812 application program from a PC so as to reconfigure the system as both an analog waveform storage scope and a digital logic analyzer. The system supports one analog channel and four digital channels, with the digital channels providing a one-level triggering. You need to write two programs: a 6812 application program and a PC host program. The 6812 application program needs to use the USB port to send data to a PC host program that displays the analog/digital waveforms simultaneously. All channels, whether analog or digital, should be sampled at the same rate. Some waveforms prior to the triggering point should also be displayed. Both the signal sampling period and the data transfer time over the USB port should be as short as possible. (Team competition!) The system should be designed so that there is no need to exit the PC host program to display a new set of samples. You must develop the system in two phases:

- Phase I: Use on-chip ADC and on-chip RAM on the MC9S12C32 chip. For this phase, the number of samples per channel can be extremely small.
- Phase II: Use off-chip ADC and off-chip RAM to store data from both types of channels.
- Alternative Phase II: Build your own USB-I2C-IO API functions and corresponding USB device drivers so that your application software can explore USB block transfer. The resulting data transfer rate should be as high as possible.

5. **Grading:** [90,100]→A, [80,90) →B, [70, 80) →C, [60, 70) →D, [0, 60) →F

(1) Lab. Project (80%) and Final Report (5%): Around two or three students work as a team, one final report per team. Grading will be based on project result, instructor's (subjective) evaluation and partners' evaluations. Team members do not necessarily get the same grade.

- A one to two page development plan (per team) is due on Jan 27. The plan should list the tasks, provide a Gantt chart for the schedule, and describe individual team member's responsibility. The project will be graded later on against the proposed schedule. There will be penalty for missing the proposed deadlines.
- The report should include an introduction section, several sections about the project, and a conclusions section. All circuit diagrams and software listings should be attached. There will be penalty on typos and grammatical errors. The length of the report should be 5 to 10 single spaced pages, excluding attachment. Lessons learned or problems encountered in the project must be documented in the report. The report will not be returned.

(2) Final (15%): March 15 (Tuesday), open book/notes; each team member is tested individually in the lab with the team's project board.